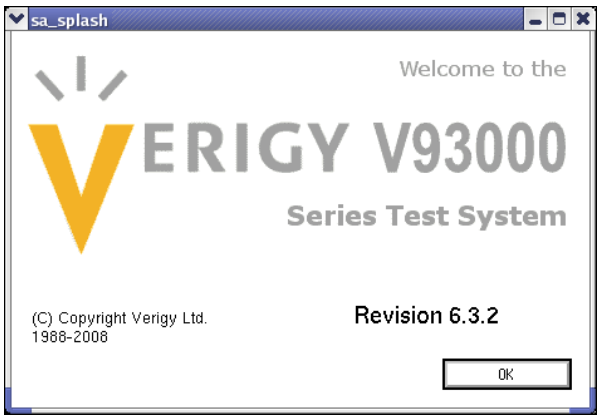
Industrial Test of Integrated Circuits

Digital Test Training on V93K ATE

LAB & EXERCISES



PART 1: DATASHEET ANALYSIS

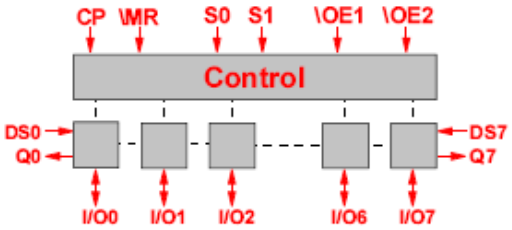
74ACT299 GENERAL DESCRIPTION

8-bit universal shift/storage register with tristate outputs.

Pin description

Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or 3-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Logic diagram



Truth table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	↗	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↗	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↗	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

- Four modes of operation controlled by (S_1, S_0)
  - hold (store)
  - shift left
  - shift right
  - load data
- Asynchronous reset controlled by $\overline{MR}$ (active on low)

DC Electrical Characteristics (ACT)

Symbol	Parameter	V_{CC} (V)	T_A = 25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5	0.0001	3.86	3.76	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL}= 24 mA
		5.5		0.36	0.44		I_{OL}= 24 mA (Note 5)
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	Minimum Dynamic Output Current (Note 6)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±3.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

AC Operating Requirements & Electrical Characteristics (ACT)

AC Operating Requirements for ACT

Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.5	ns
t_H	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	−2.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.0	ns
t_H	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	−1.0	1.0	1.0	ns
t_W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns
t_W	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	3.5	ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	5.0	0	1.5	1.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Input Frequency	5.0	120	170		110		MHz
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
t_{PLH}	Propagation Delay CP to I/O_n	5.0	4.5	8.5	12.5	4.5	13.5	ns
t_{PHL}	Propagation Delay CP to I/O_n	5.0	5.0	9.5	15.0	4.5	16.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	4.0	14.0	15.0	4.0	18.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0	4.0	13.0	14.5	3.5	17.5	ns
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.5	8.0	12.0	1.5	13.0	ns
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.0	8.0	12.0	1.5	13.5	ns
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0	2.0	8.5	12.5	2.0	13.5	ns
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0	2.5	8.0	11.5	2.0	12.5	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

1. Exercise: 74ACT299 – Test patterns for functional test

Referring to the truth table, fill missing instructions in the right column and complete the test vector columns for each pin when necessary (remember that no empty entries are allowed).

MR	CP	S0	S1	DS0	DS7	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	Q0	Q7	INSTRUCTIONS
0	1	0	0	1	1	1	1	1	1	1	1	1	1	X	X	Reset
1	1	0	0	1	1	L	L	L	L	L	L	L	L	L	L	Hold
1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L	// Load 10000000
1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L	
1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L	
1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H	
1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L	
1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H	Shift left 1
																Shift left 1
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
																Shift left 0
1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L	Hold
																// Load 10101010
																Hold
																Shift right 0
																Hold
																Reset
1	1	1	1	0	0	1	1	1	1	1	1	1	1	H	H	// Load 11111111
1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L	
1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L	

Now you have to write a test pattern which first makes device initialization and verifies the correct initialization, then makes a parallel load all IOs at “1”, and finally verifies the shift left function with the serial input DS7 set at “0” until a “L” state can be read out on the serial output Q0.

MR	CP	S0	S1	DS0	DS7	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	Q0	Q7	INSTRUCTIONS

2. Exercise: 74ACT299 – Values for parametric tests

Referring to DC electrical characteristics, extract the value guaranteed in the datasheet for the following parameters. The conditions are T=25°C and Vcc=4.5V.

Datasheet guaranteed value	
Vil =	
Vih =	
Vol =	with iol=24mA & Vcc=4.5V
Voh =	with ioh=-24mA & Vcc=4.5V

Referring to AC operating requirements and AC electrical characteristics, extract the value guaranteed in the datasheet for the following parameters when T=25°C and Vcc=5V.

Datasheet guaranteed value
Setup time I/O vs CP =
Setup time DS0/DS7 vs CP =
Setup time S0/S1 vs CP =
Hold time I/O vs CP =
Hold time DS0/DS7 vs CP =
Hold time S0/S1 vs CP =
Propagation delay I/O vs CP =
Propagation delay Q0/Q7 vs CP =

.PART 2: TESTER HW/SW & BASIC ELEMENTS

FIRST STEPS WITH SMARTEST: PART 1

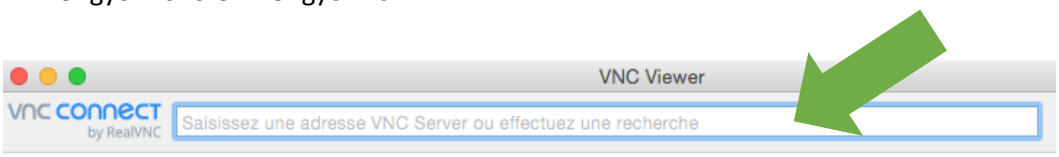
Step 1: Launching SmarTest

1/ Open the VNC icon 

Ask the teacher your login and refer to the following table to get your password, the VNC display number and the default machine M to use for offline connection.

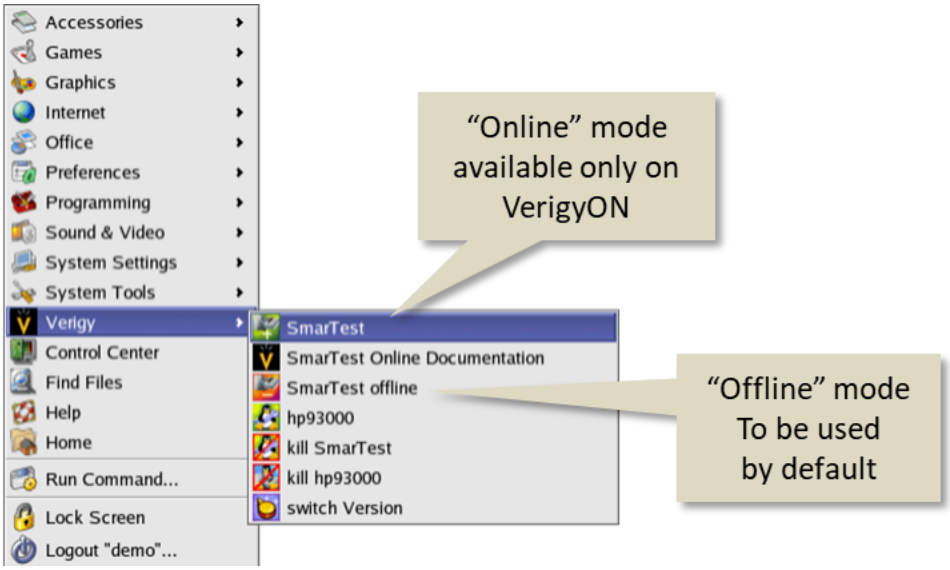
Login trainXv93	**Password #trainXv93#**	**Y: VNC display number**	**M: Default machine for offline connection**
train1v93	#train1v93#	71	verigyon2016
train2v93	#train2v93#	72	verigyon2016
train3v93	#train3v93#	73	verigyoff2017
train4v93	#train4v93#	74	verigyoff2017
train5v93	#train5v93#	75	verigyoff2017
train6v93	#train6v93#	76	verigyoff2017
train7v93	#train7v93#	77	verigyoff2017
train8v93	#train8v93#	78	verigyoff2017

2/ Use this information to fill the VNC Connect window: **M.cnfm.fr:Y**
with **M** = verigyon2016 **OR** verigyoff2017

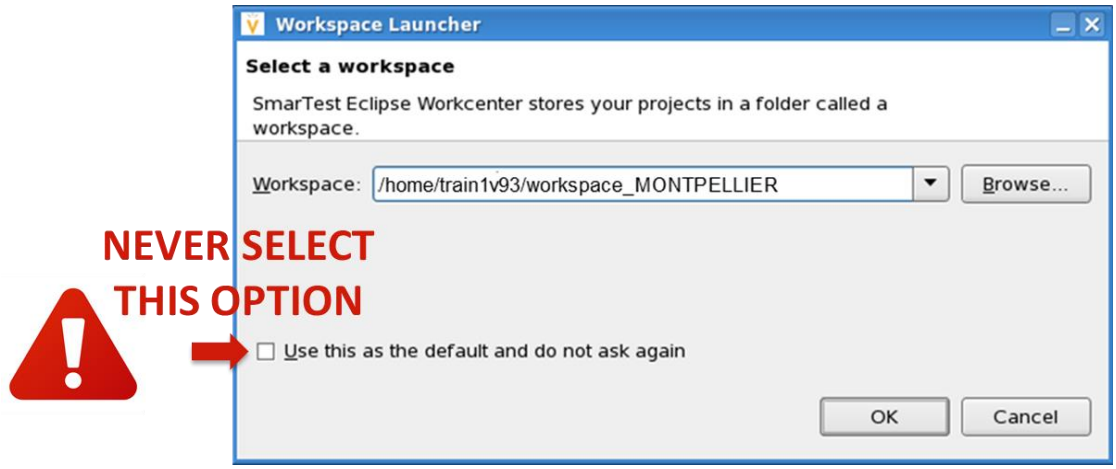


Once the connection established, according to the machine you connected, you should get one of the 2 following windows.

3/ From the start menu «  » (also called RedHat menu), the shortcuts to launch **SmarTest®** are located in the menu "**Verigy**" or "**Advantest**".



When starting **SmarTest®**, you will have displayed a window called Workspace Launcher window. Select Ok if you have the following path: ***/home/trainXv93/workspace_MONTPELLIER***; otherwise "Browse" through the directories to access it.

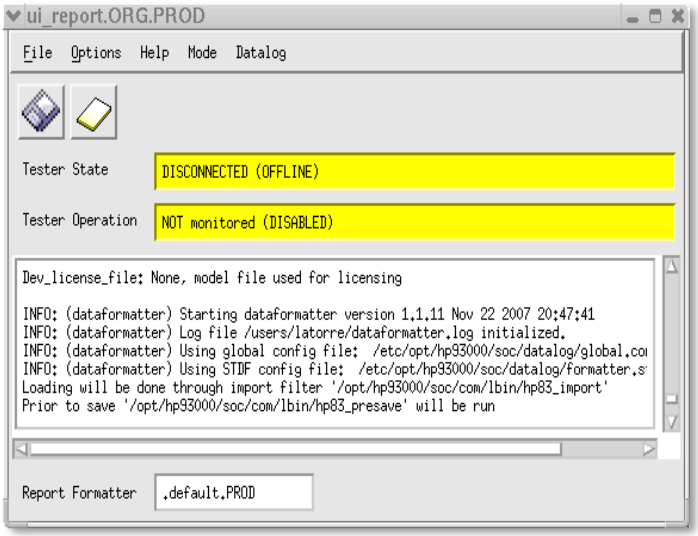


Never save your test program under this path. This is not the expected test program directory. It will induce errors.

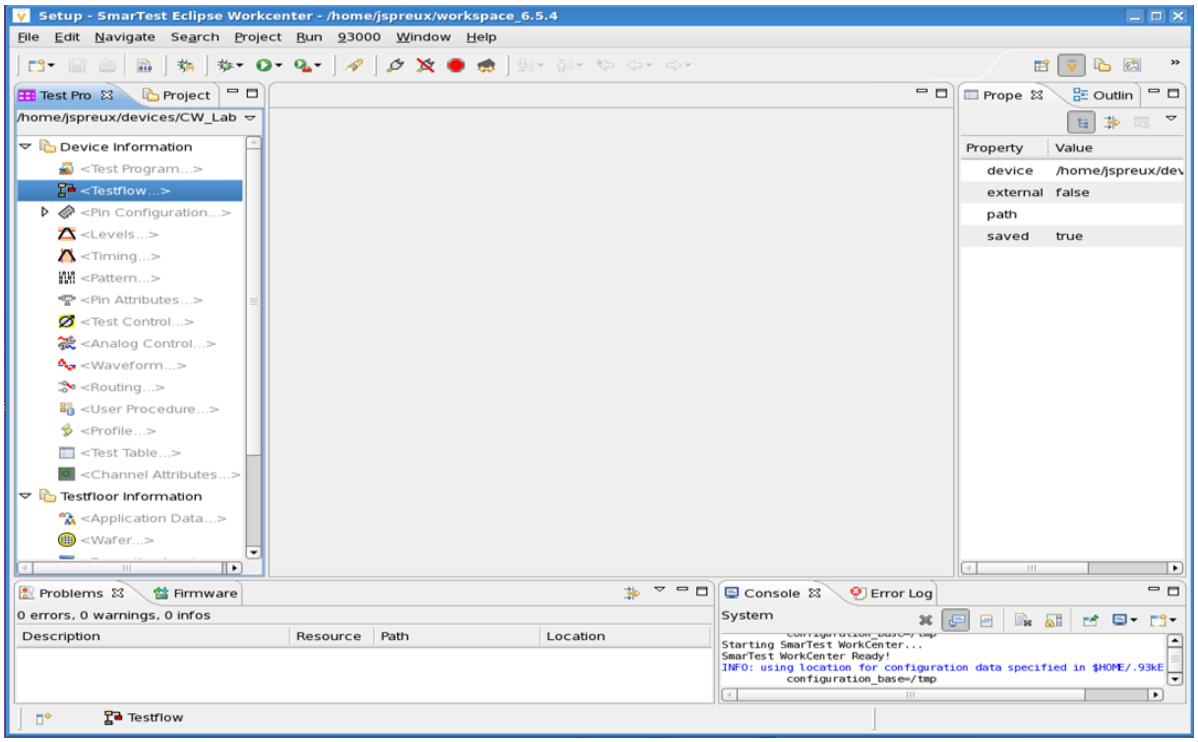
When launching **SmarTest®**, 3 windows appear on the screen:

- « **Operation Control** » window allows controlling tasks execution on tester.
  Used to format datalog stream results.

- « **ui_report** » window allows following the communication between the tester and **SmarTest®**. It is very important to regularly look at this window to verify if any error or warning messages appear.

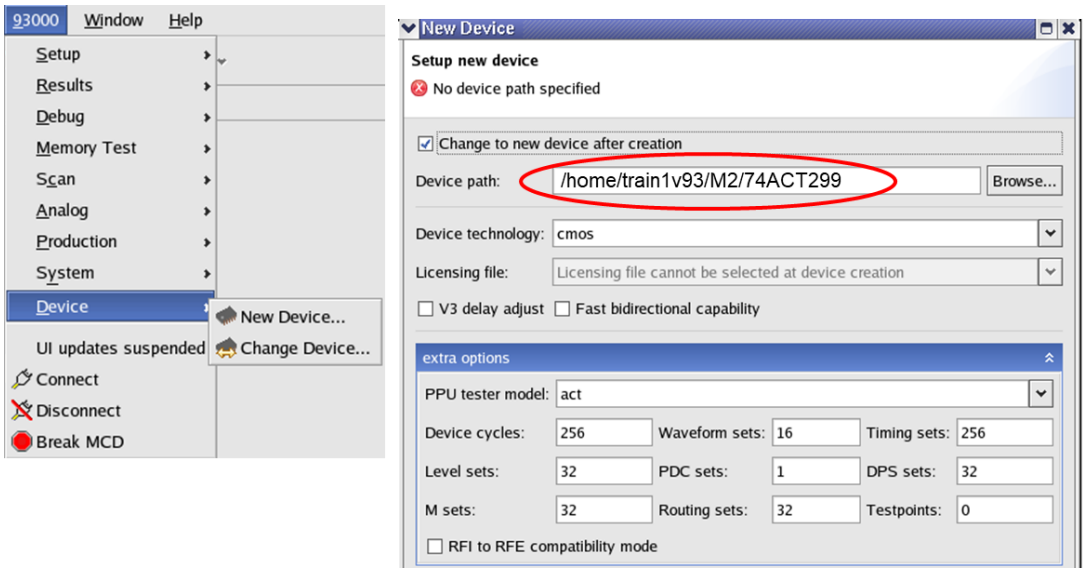


- « **SmarTest Eclipse Workcenter** » window where the users will find all tools to develop a test program.



Step 2: Creating SmarTest Device directory

From the tool bar of the “Smartest Eclipse Workcenter” window, select **93000/Device/New Device**; from the opened window, browse the path **/home/trainXv93/M2/** and enter the name **74ACT299** to create the new test program directory (refer to picture below).

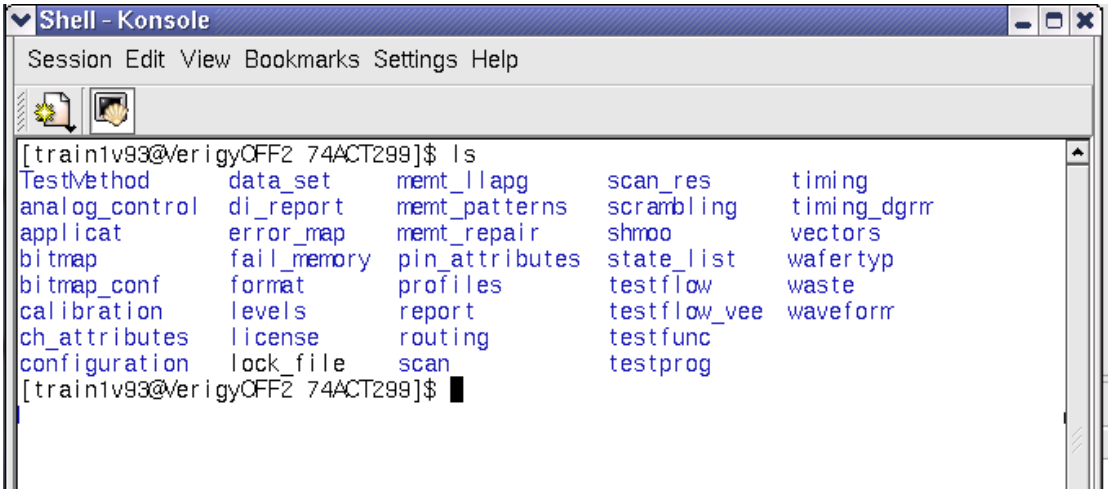


Return to the RedHad menu and open a “Terminal” window from “**System Tools**”.

Type the following command to access to your device directory:

> cd /home/trainXv93/M2/74ACT299

> ls (to see all the sub-directories automatically created)



Reminder: Procedure to exit SmarTest and VNC

- *Exiting **SmarTest**: click **“File > Exit”***
- *Exiting **VNC**: click on the **cross** ☒ **(DO NOT LOGOUT!)***

FIRST STEPS WITH SMARTEST: PART 2

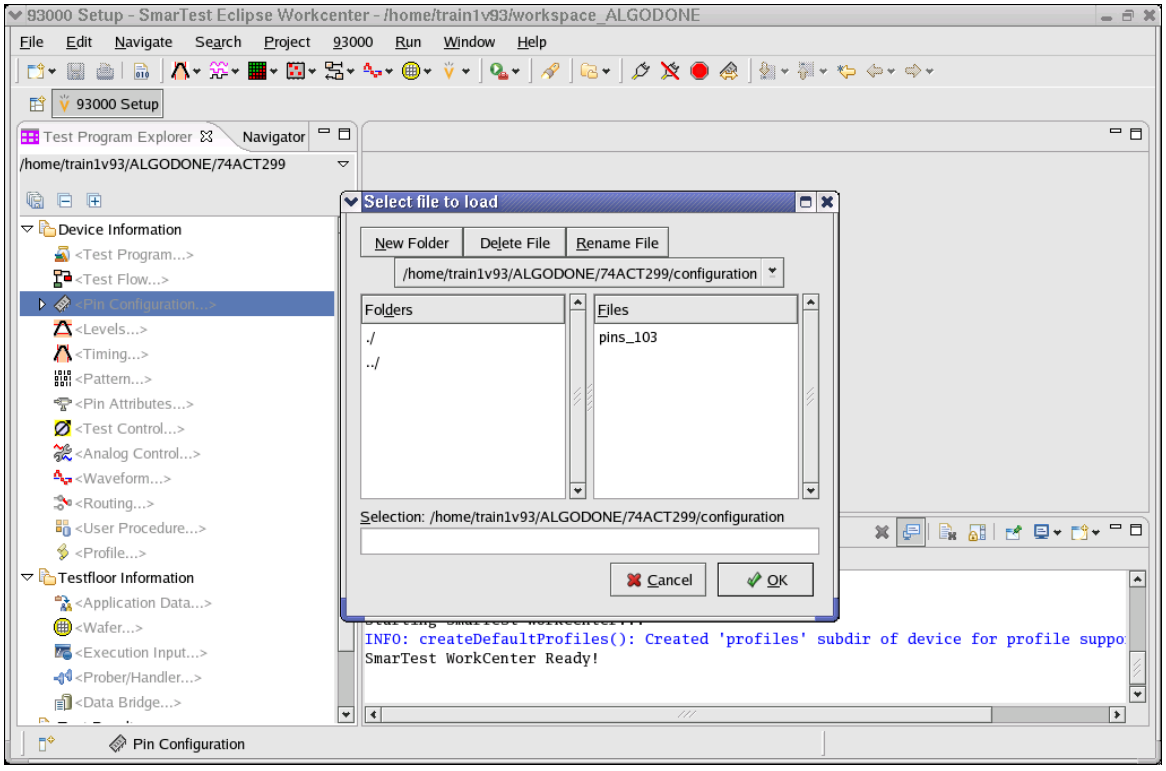
Now, you are going to setup the basic elements: PINS, LEVELS, TIMING, PATTERN.

Step 1: PINS

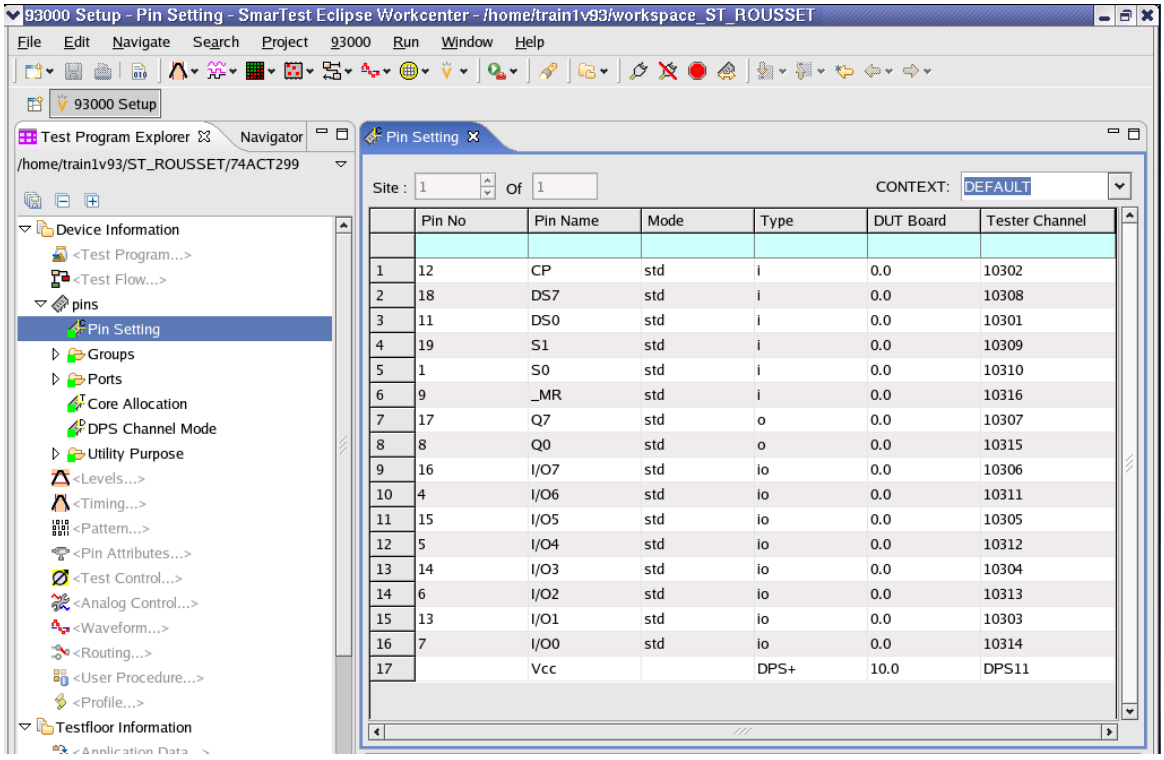
Depending on the progress of the course, the pin configuration will be either created by the trainees or given by the trainer.

To copy an existing pin configuration file:

- OPEN a terminal window.
- Type the following command:
  > cp /home/trainer/74ACT299/INIT_FILES/pins_103 /home/trainXv93/M2/74ACT299/configuration/.
- From the **Test Program Explorer** window on **SmarTest**, select the “**Pin Configuration**” grey item (grey means not loaded). From the right click menu, load this “Pin Configuration” file.



Have a look at the pins and pin groups setup:



Step 2: LEVELS

Repeat the operation for the levels:

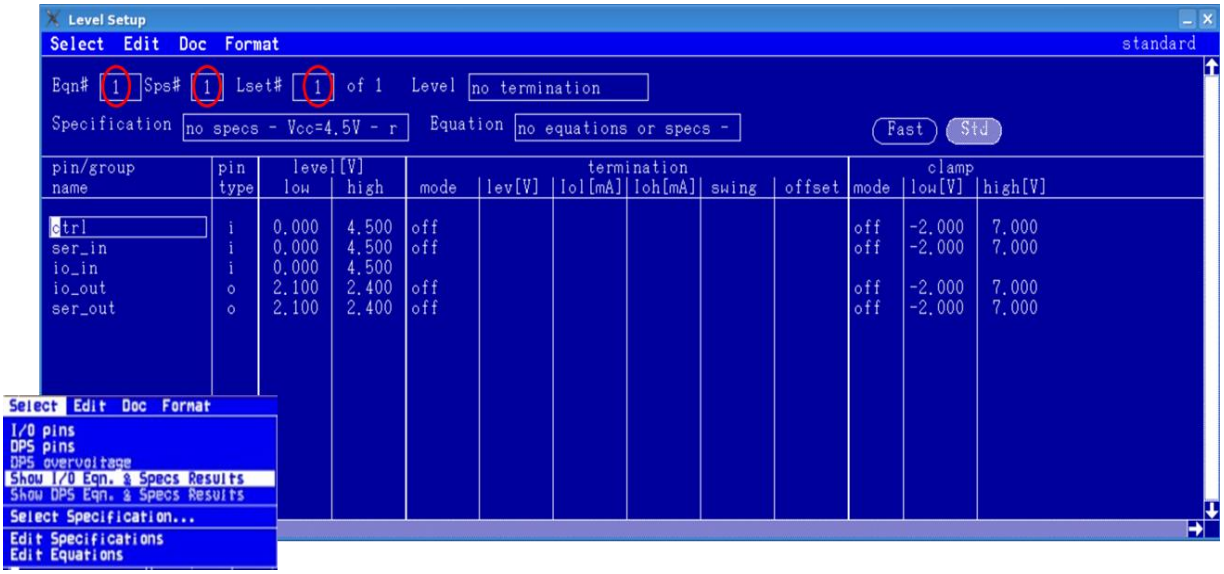
- Copy an existing levels file to your device level directory with the command:

  > cp /home/trainer/74ACT299/INIT_FILES/levels_74ACT299 /home/trainXv93/M2/74ACT299/levels/.

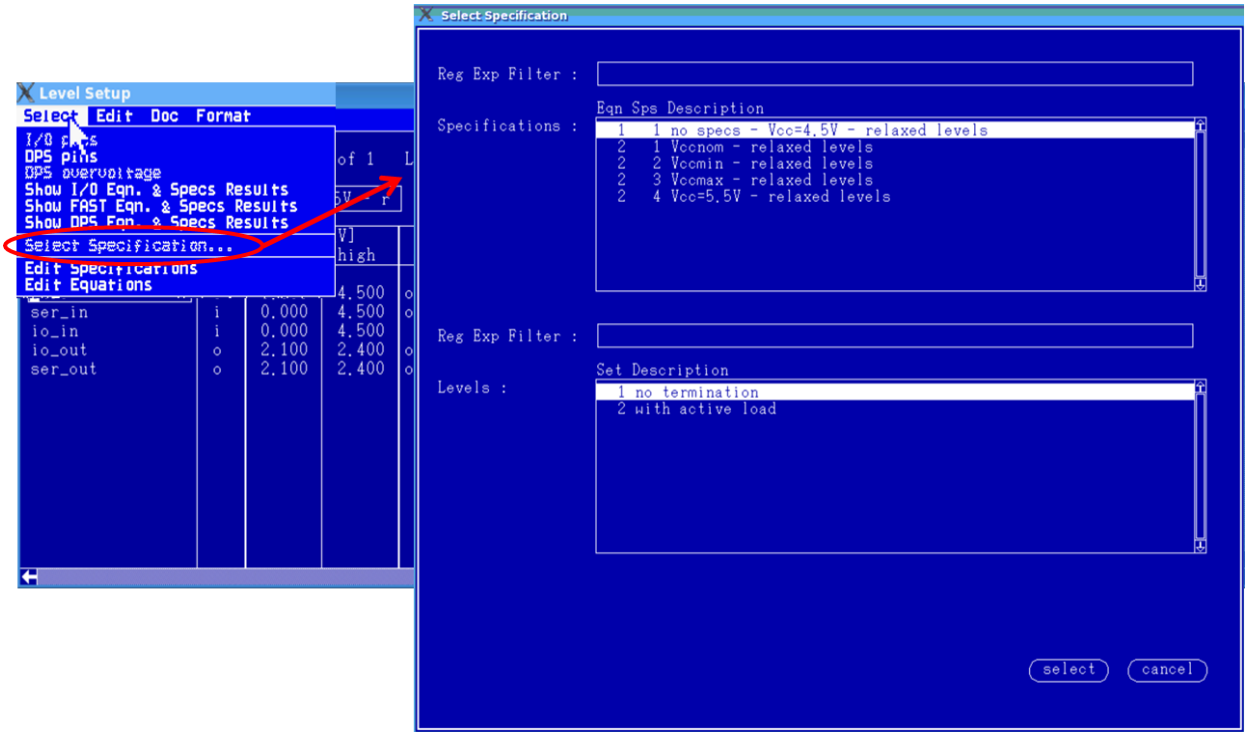
- Return to the Test Program Explorer and load the levels:
  1. From the Test Program Explorer, select "**levels**" item
  2. From the right click menu, select "**Load**"
  3. From the "Select File to Load" window, select "**levels_74ACT299**"

- Open the Level Setup window from the level item in the Test Program Explorer (« open » from the right-click menu or double-click). Displayed values are defaults values.

From the menu "**Select**" of the Level Setup window, choose "**Show I/O Eqn & Specs Results**" to display the levels that will be applied to the device as specified by Eqn#, Sps# and Lset#.

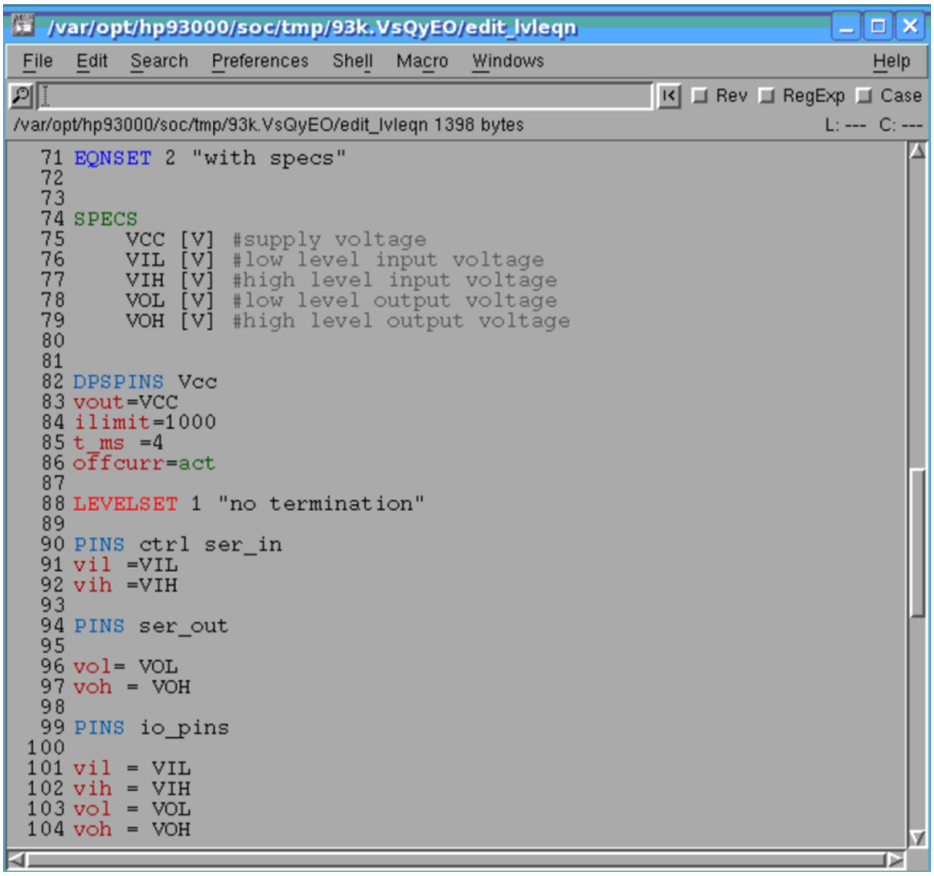


You can access to the list of existing Eqn#, Sps# and Lset# from the menu "**Select->Select Specification…**" and choose the one you want to display.

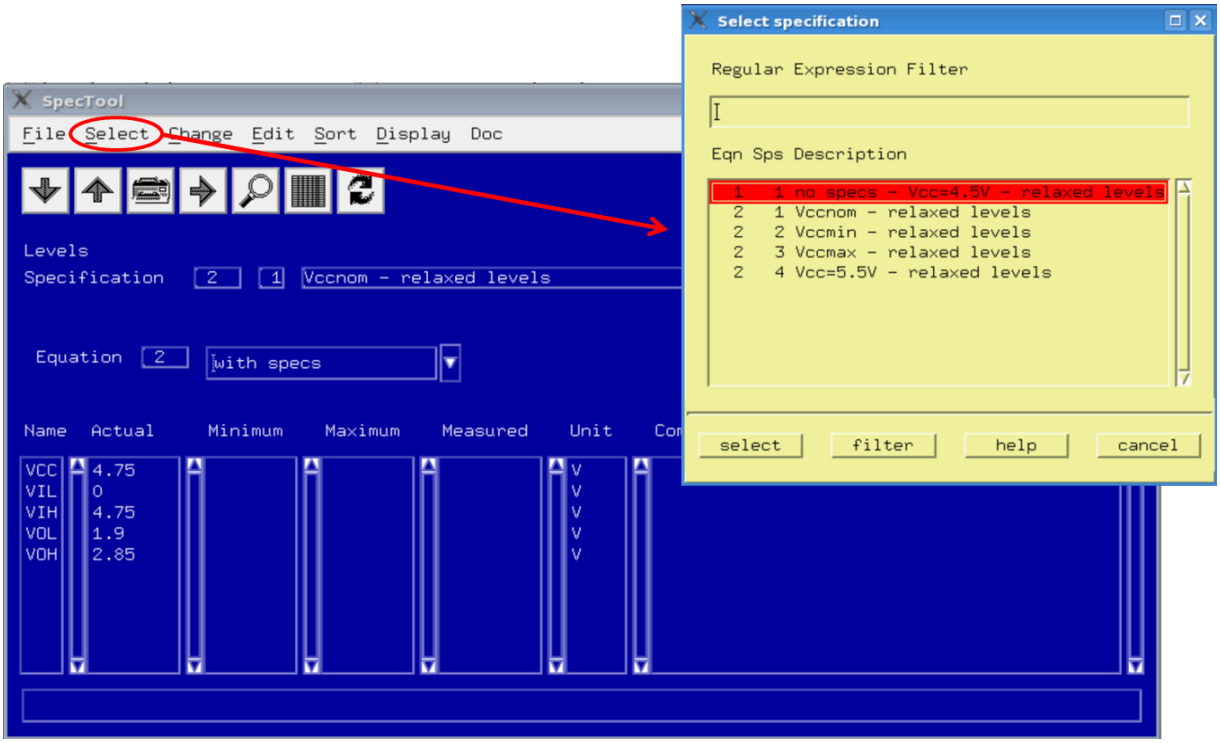


To understand how these values have been programmed:

- Choose "**Edit Equations**" from the menu "**Select**" to open the Level Equation Set Editor; look at the defined EQNSETs and LEVELSETs.



- Choose “**Edit Specifications**” from the menu “**Select**” to open the Spec Tool; look at the Spec Variables and their values for the different SpecSets.
  Use the menu “**Select**” of the **Spec Tool** to choose among the list of existing specifications with their description the one you want to display in the Spec Tool.



Exercise: 74ACT299 – Basic Elements - Levels

Using the tools/editors available in SmarTest, find the information to fill in the following table.

Eqn #	Spec #	Lset #	supply	all_in		all_out		
			DPS value	Drive values		Compare values		Active Load?
				low	high	low	high	
1	1	1						Yes/No
1	1	2						Yes/No
2	1	1						Yes/No
2	2	1						Yes/No
2	3	1						Yes/No

Step 3: TIMING

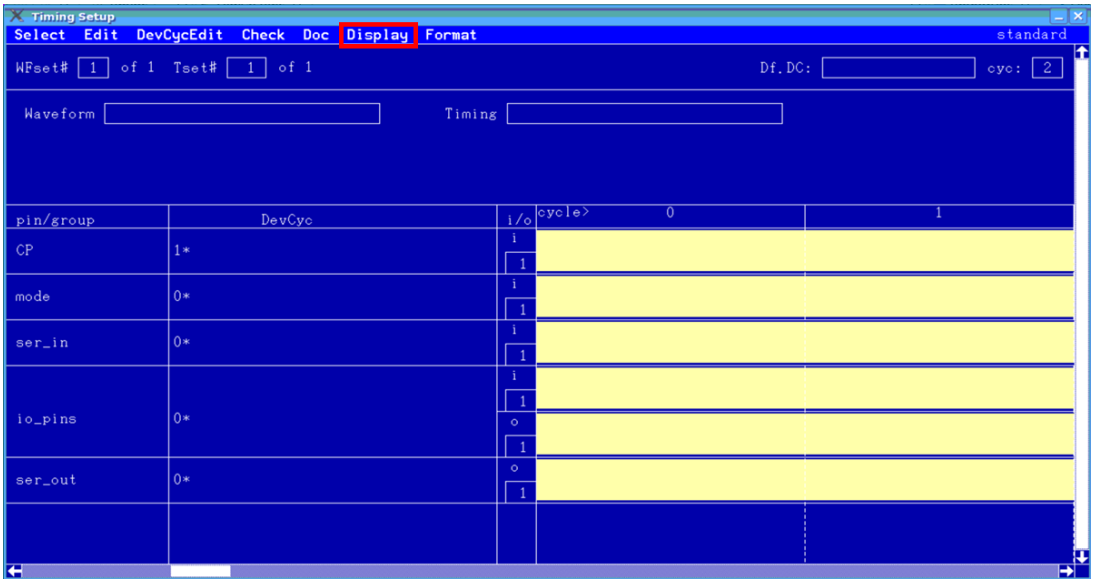
Repeat the operation for the timing:

- Copy an existing timing file to your device level directory with the command:

  > cp /home/trainer/74ACT299/INIT_FILES/timing_74ACT299 /home/trainXv93/M2/74ACT299/timing/.

- Return to the Test Program Explorer and load the timing:
  1. From the Test Program Explorer, select "**timing**" item
  2. From the right click menu, select "**Load**"
  3. From the "Select File to Load" window, select "**timing_74ACT299**"

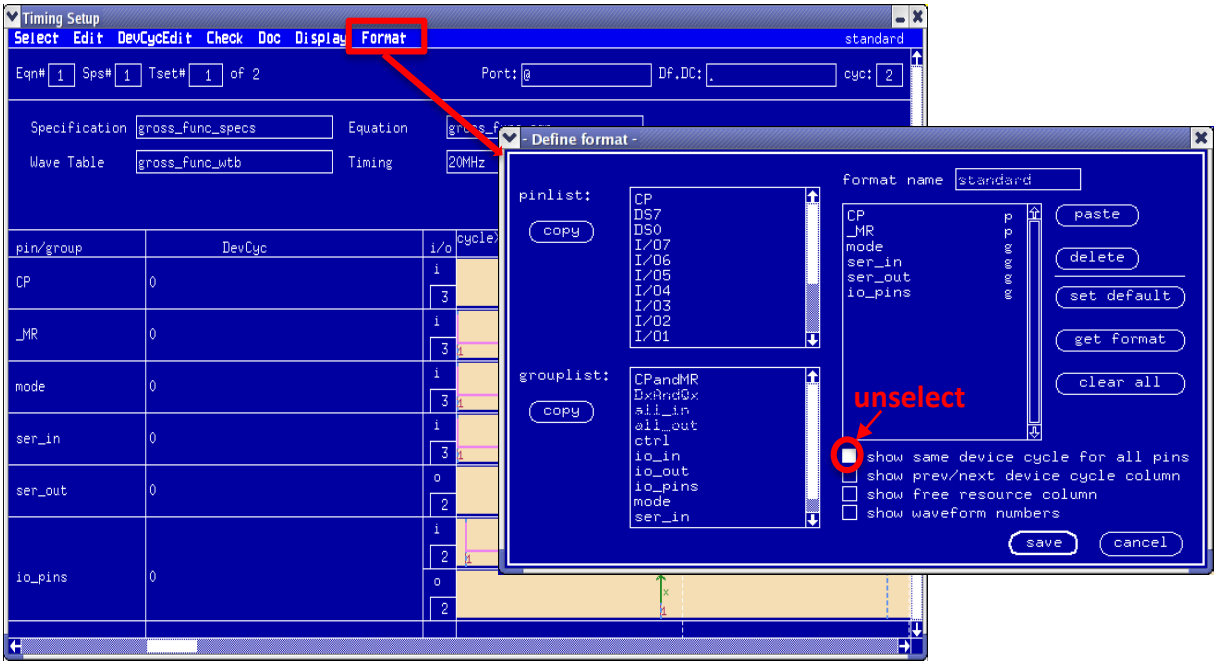
- Open the Timing Setup window from the timing item in the Test Program Explorer ("open" from the right-click menu or double-click).



Select "DISPLAY->DOUBLE" to enlarge the window.

Create an appropriate format to visualize the waveforms for the different types of pin:

- from the menu "**Format**", choose "**new**"
- define a format that contains CP, _MR, mode, ser_in, ser_out, io_pins
- **unselect** the box "show same device cycle for all pins"
- **save** your changes



The Timing Setup window now shows one waveform for each pin or pin group defined in the format, as specified by Eqn#, Sps# and Tset#. If it is not the case, choose "**Show Eqn & Spec Results**" from the menu "**Select**" and fill the device cycle name you want to display for each pin or pin group in the "DevCyc" column.

To see all the waveforms defined for a given pin or pin group, click on the name of a pin or pin group and choose "**One pin**" from the menu "**Select**". It will show you all the defined waveforms for the chosen pin or pin group.

To see again all pins or pin groups, choose again "**format pins**" from the menu "**Select**".

To see the values of edge location for a given pin or pin group, click on the name of a pin or pin group and choose "**Edge delay**" from the menu "**Select**". It will show you the value of defined edge delays for the chosen pin or pin group.

Note: You can access to the list of existing Eqn#, Sps# and Tset# from the menu "**Select->Select Specification…**" and choose the one you want to display.

To understand the waveforms displayed in the Timing Setup window:

- look at the waveform table ("**edit wave tables**" from the menu "**Select**")
- look at the definition of edges location ("**edit equations**" from the menu "**Select**")
- look at the values of the spec variables ("**edit specifications**" from the menu "**Select**")

Exercise: 74ACT299 – Basic Elements - Timing

Using the tools/editors available in SmarTest, find the information to answer the following questions.

Case 1: Eqn# 1, Spec# 1, Tset# 1
Case 2: Eqn# 1, Spec# 1, Tset# 2
Case 3: Eqn# 2, Spec# 1, Tset# 1
Case 4: Eqn# 2, Spec# 2, Tset# 1
Case 5: Eqn# 3, Spec# 1, Tset# 1

Which case do not comply with the propagation delay time I/O vs CP given in the datasheet (refer to the value you have extracted from the datasheet, page 6 of this document). Justify your answer.

Which case has the correct waveform format to verify setup or hold times? Justify your answer.

Step 4: PATTERN

Repeat the operation for the pattern:

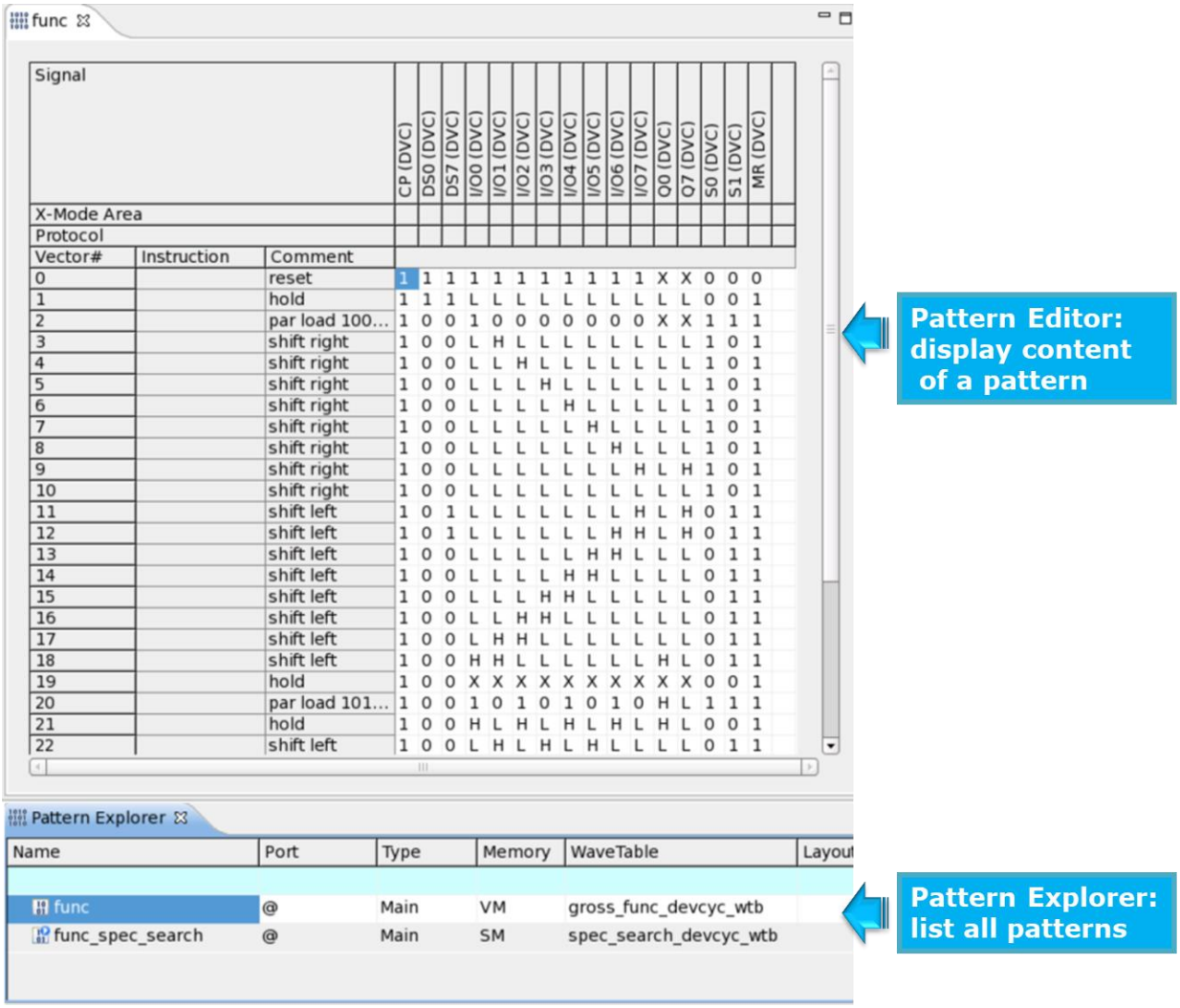
- Copy an existing pattern file to your device level directory with the command:

  > cp /home/trainer/74ACT299/INIT_FILES/pattern_first_flow /home/trainXv93/M2/74ACT299/vectors/.

- Return to the Test Program Explorer and load the pattern:
  4. From the Test Program Explorer, select "**pattern**" item
  5. From the right click menu, select "**Load**"
  6. From the "Select File to Load" window, select "**pattern_first_flow**"

From the Test Program Explorer, double-click on "pattern_first_flow" to display the pattern list in **Test Pattern Explorer window**.

For this example, the pattern list only contains 2 patterns.
Double-click on the pattern called "**func**" and look at the detail of this pattern in the **Pattern Editor** (you should recognize the pattern from the first exercise).



Reminder: Procedure to exit SmarTest and VNC

- *Exiting **SmarTest**: click **"File > Exit"***
- *Exiting **VNC**: click on the **cross** ☒ **(DO NOT LOGOUT!)***

PART 3:

QUESTIONS ABOUT FIRST TEST CONCEPTS

Answer to the following questions relative to the test concepts.

Continuity test

What is the purpose of this test?

What is the voltage applied on Vcc and device pins? Why?

The measured voltage on a given pin is 0.004V.
What does it mean for this pin?

The measured voltage on a given pin is 2.0V.
What does it mean for this pin?

Gross IDD test

What is the purpose of this test?

What is the voltage applied to Vcc?

What are the voltages applied on inputs for low and high levels?

Referring to DC electrical characteristics, what is the guaranteed limit value for the standby current (at T=25°C)? Indicate whether it is a min or a max value.

Functional/Structural test

What are the voltages applied on inputs for low and high levels in case of a relaxed functional test?

What are the comparator threshold voltages typically used for interpretation of low and high levels in case of a relaxed functional test?

What are the main differences and similarities between structural and functional test approaches?

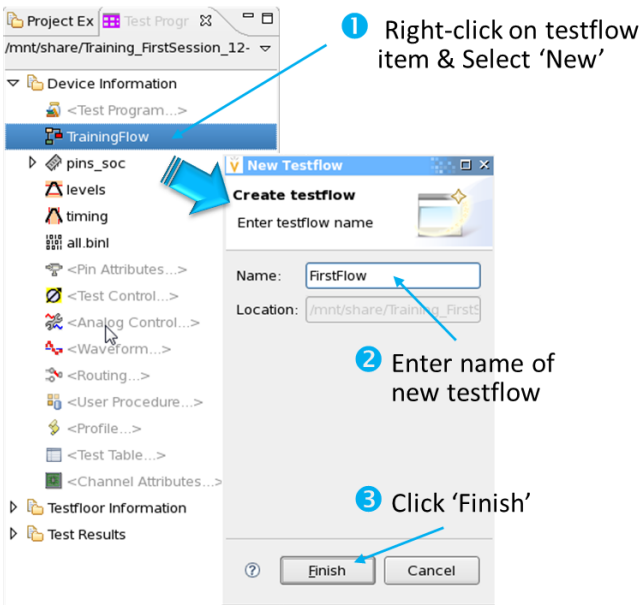
PART 4: TEST PROGRAM

TEST PROGRAM DEVELOPMENT: FIRST TEST FLOW

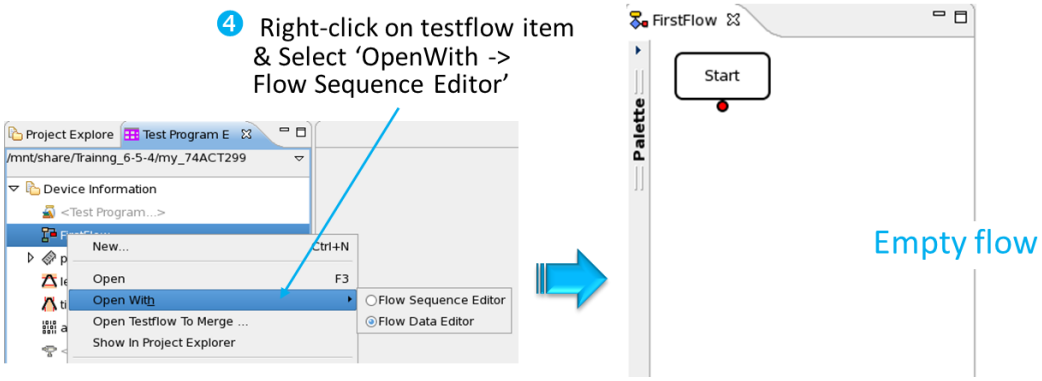
Step 5: Create your first test flow

From the **Test Program Explorer** (Setup Perspective), select the "**Testflow"** item. To create a new test flow, perform the following actions:

- From the right click menu, select **"New"**.
- Enter the testflow name **"first_flow"** and click **"Finish"**.



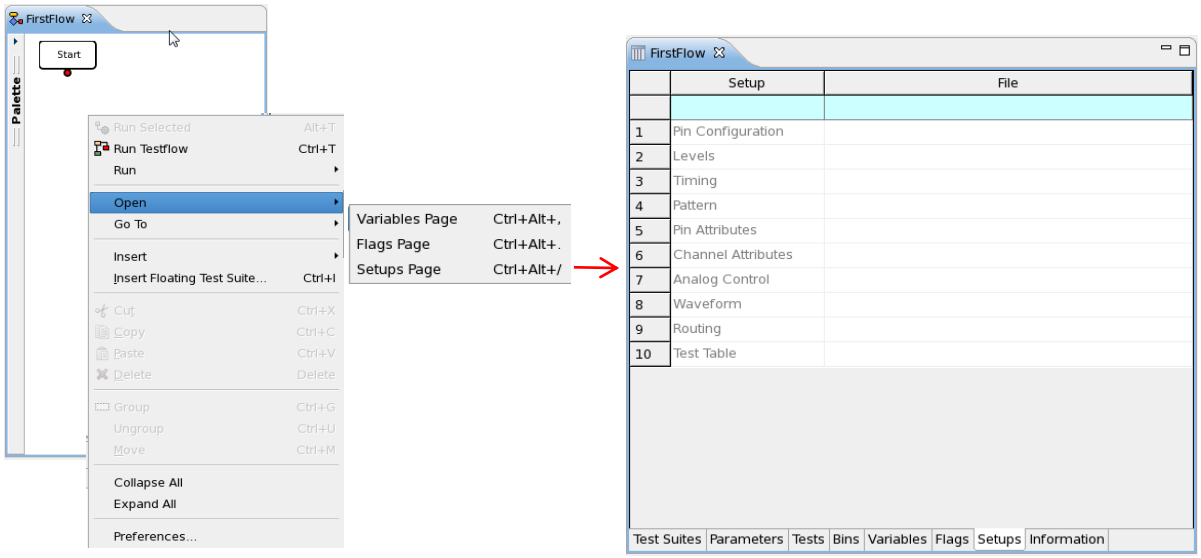
- From the right click menu on the Testflow item, select **"Open with > Flow Sequence Editor"**. An empty flow is opened in the flow sequence editor.



Step 6: Setup the context

The next step is to setup the context, i.e. to specify the pins, levels, timing and pattern that will be associated to this test flow. For this, perform the following actions:

- Right-click in an empty zone of the testflow window and select **"Open > Setups Page"**.
- Fill-in your primary files in the corresponding setup entry (pins_103, levels_74ACT299, timing_74ACT299, pattern_first_flow).



- Return to Test Program Explorer, select the "**Testflow"** item and select **"Load All Setups"** from the right click menu.

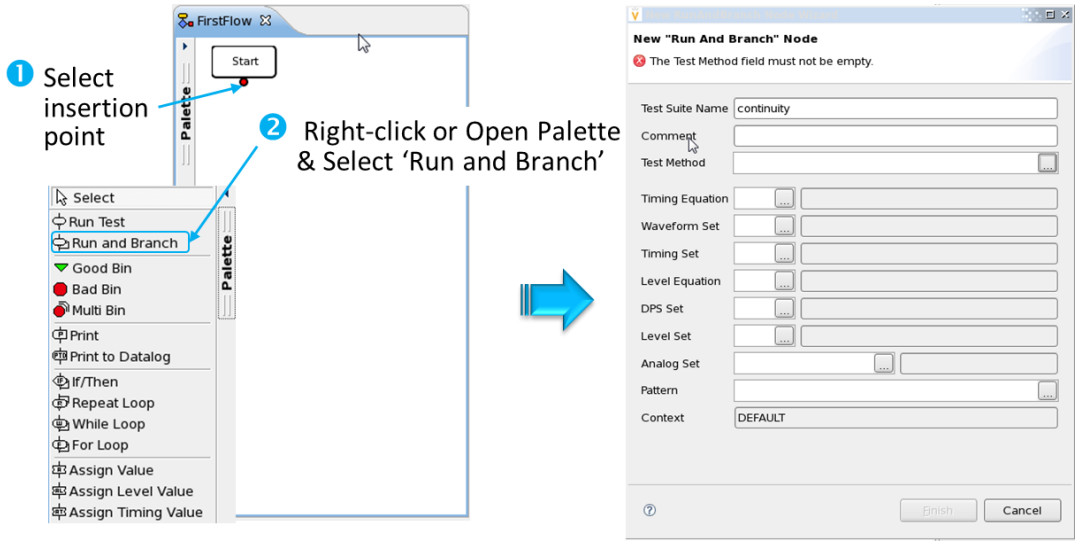
Step 7: Insert Testsuites

Now you have to insert a test block for each test you want to perform. For this first test flow, you have to implement **4 tests**:

- a continuity test
- a functional test @Vccmin
- a functional test @Vccnom
- a functional test @Vccmax

To insert a new Testsuite, perform the following actions:

- Choose the insertion point and select **"Insert** > **run and branch"** from the right click menu
- Fill in the required information and click **"Finish"**.



Details on the required information for continuity and functional test blocks are given herafter (choices for timing and pattern information are given but **you have to make the appropriate choices regarding level information for each test block**).

Continuity test

TESTSUITE FIELDS	VALUE
Testsuite name	Continuity
Timing Equation	1
Timing Spec Set	1
Timing Set	1
Level Equation	**Choose the appropriate Level Equation**
Level Spec	**Choose the appropriate Level Spec**
Level Set	**Choose the appropriate Level Set**
Pattern	"func"

In the **"Test Method"** line:
select "**dc_tml>DcTest>Continuity"** and click **OK**.

Functional test

TESTSUITE FIELDS	VALUE
Testsuite name	Functional_Vccmin/nom/max
Timing Equation	1
Timing Spec Set	1
Timing Set	1
Level Equation	**Choose the appropriate Level Equation**
Level Spec	**Choose the appropriate Level Spec**
Level Set	**Choose the appropriate Level Set**
Pattern	"func"

In the **"Test Method"** line:
select "**ac_tml** > **AcTest** > **FunctionalTest"** and click **OK**.

Exercise: 74ACT299 – First Test Flow – Level choices

Test Block	Level Equation #	Level Spec #	Level Set #
Continuity			
Functional@Vccmin			
Functional@Vccnom			
Functional@Vccmax			

Step 8: Insert Bins

You have now to insert a bad bin in the failing branch of each test block and a good bin at the end of the test flow according to the information given in the following table.

BIN TYPE	INSERTION POINT	SOFT BIN #	SOFT BIN NAME	HARD BIN #	HARD BIN NAME
BAD	CONTINUITY Failing Branch	2	FAILED CONTINUITY	2	CONTINUITY
BAD	FUNCTIONAL Vccmin Failing Branch	3	FAILED FUNCTIONAL Vccmin	3	FUNCTIONAL
BAD	FUNCTIONAL Vccnom Failing Branch	4	FAILED FUNCTIONAL Vccnom	3	FUNCTIONAL
BAD	FUNCTIONAL Vccmax Failing Branch	5	FAILED FUNCTIONAL Vccmax	3	FUNCTIONAL
GOOD	FUNCTIONAL Vccmax Passing Branch ***(end of test flow)***	1	PASS	1	PASS

To insert a new Bin, perform the following actions:

- Choose the insertion point and select **"Insert** > **Good/Bad Bin"** from the right click menu.
- Fill in the required information and click **"Finish"**.

Step 9: Define parameters and limits

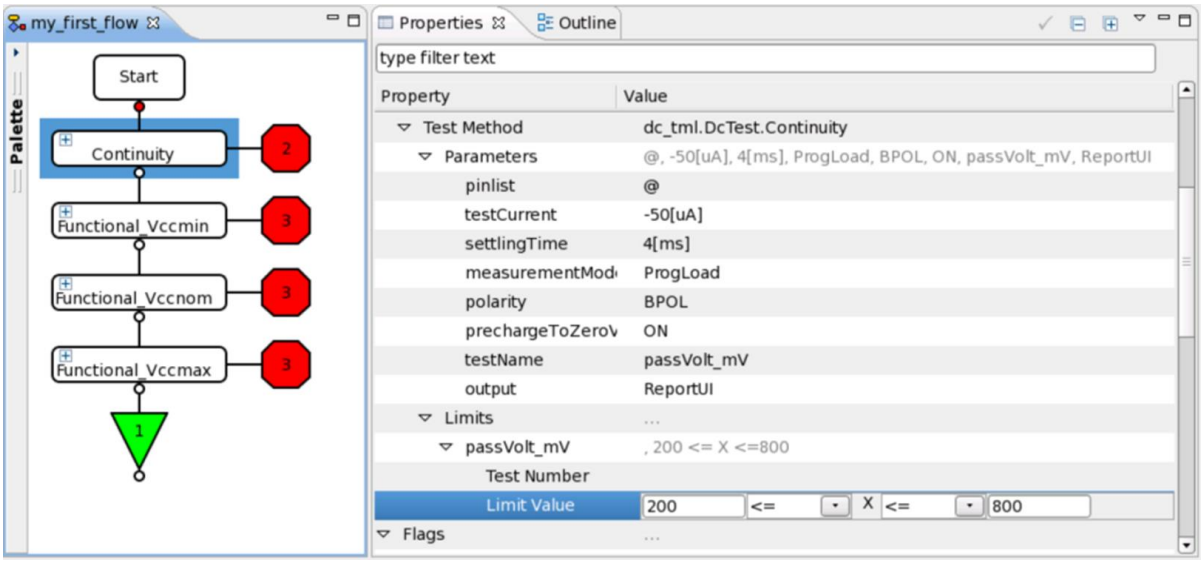
You have to setup the test conditions and limits of your **continuity test block** according to the following information.

Field	Value	Comment
pin list	@ all pins	
test current	–50	uA
pass volt min	200	mV
pass volt max	800	mV
settling time	4	ms
measurement mode	PPMUpar/ProgLoad	*(your choice)*
polarity	SPOL/BPOL	*(your choice)*
output	ReportUI	

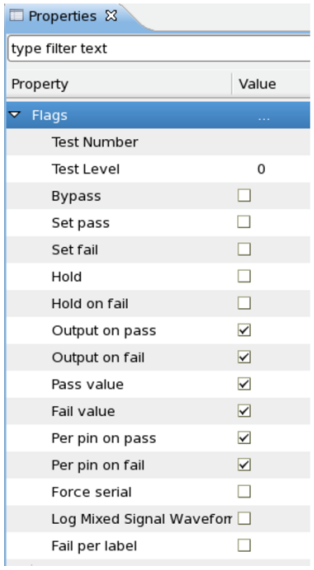
Practically to setup the test conditions and limits of a Testsuite, perform the following actions:

- Double-click on the Testsuite in the Test Flow Editor; the Properties View opens.
- In the **Properties** widow, unfold **"Test Methods"** (see figure herafter)
    - Unfold **"Parameters"** and replace default values by yours.
    - Unfold **"Limits"** and replace default values by yours.

Caution: Do not write the units when entering values.



Functional test block takes no test conditions and no test limits (except the pinlist), so you don't have to change the default values.



Step 10: Flag setting and test execution (offline)

The final step before test execution is to set flags for each Testsuite to specify which results will be displayed in the UI-Report window.

For this, go to the **Properties** view of each Testsuite, unfold "**Flags"** and activate the following options:

- Output on pass
- Output on fail
- Pass value
- Fail value
- Per pin on pass
- Per pin on fail

The tests are now ready to be executed. You have 2 options from the Testflow editor:

1. Select a Testsuite and choose **"Run Selected"** from the right click menu. Only this test block is executed.
2. Click on any zone of the test flow and choose **"Run Testflow"** from the right click menu. The complete test flow is executed.

Try both these options and look at the UI-Report window to make sure you have no syntax error and to visualize the displayed results. (Clear the Report window before each execution).

Note: In the offline mode, the Continuity test fails because the simulator returns 0 value for the measured pin voltage. To execute the complete test flow despite this fail, activate the Flag "**Set Pass**" of the continuity test in the **Properties** window. You should obtain a Pass when running the complete test flow.

Your first test flow is now complete and ready to be verified online. For this, quit the simulator mode and connect online to the tester.
Do not forget to disable the Flag "Set Pass" of the continuity test before going to the online mode.

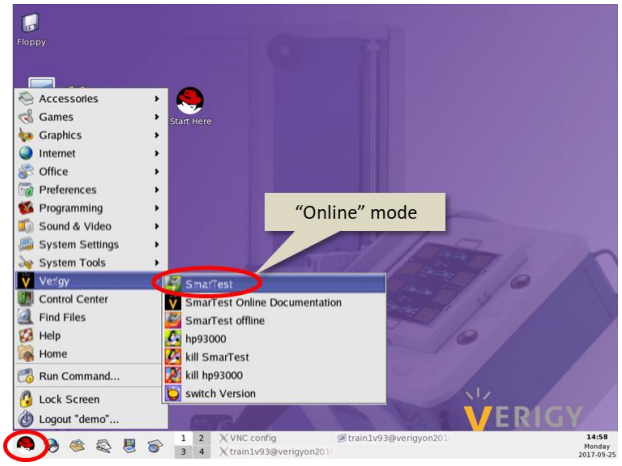
Reminder: Procedure to exit SmarTest and VNC

- *Exiting **SmarTest**: click **"File > Exit"***
- *Exiting **VNC**: click on the **cross** ☒ **(DO NOT LOGOUT!)***

Step 11: Online test execution

Connect to the online machine **verigyon2016** using VNC. Keep the same login and password (cf. page 7 to remember your password and VNC display number).

Once the VNC window is opened (purple background), start the online license from the RedHad menu : **"Verigy >SmarTest"**



In the Test Program Explorer window, check that the test program path is yours (/home/trainXv93/M2/74ACT299). Otherwise, click **"93000 > Device > Change Device"** and select the path relative to your test program.

From the Test Program Explorer, load your test flow (first_flow) and all the primary files (pins_103, levels_74ACT299, timing_74ACT299, pattern_first_flow).

Open your test flow in the Flow Sequence Editor and perform the following experiments:

1. Execute the complete test flow and verify you obtain a PASS.
2. Execute only the continuity test and look at the results in the UI-Report window. Do you understand them?
3. Return to the **Properties** window of the continuity test and change the "**Polarity**" in the "**Parameters**" section. Execute the test and look at the results in the UI-Report window. Do you understand them?
4. Return to the **Properties** window of the continuity test and change the **"MeasurementMode"** in the "**Parameters**" section. Execute the test and look at the results in the UI-Report window. Do you understand them?
5. Execute only a functional test and look at the results in the UI-Report window. Do you understand them?

PART 5: TEST METHODS

IMPLEMENTATION OF PARAMETRIC TESTS on 74ACT299

In this lab, you will run a more thorough test flow that includes not only continuity and functional tests but also some DC and AC parametric tests. The structure of the test flow will be provided.
The objective of the exercise is to define the test conditions and limits of the parametric tests according to the device datasheet and to evaluate the actual circuit performances.

Note: to know which test conditions and/or test limits you have to change in each test block, return to page 6 of this document and consult the values you have extracted from the data sheet

Step 1: Copy an existing test flow and its associated primary files (offline)

- Open a terminal window from the RedHat menu «  ».
- Copy the test flow file called "**full_flow_2Modify**" to your "testflow" directory with the command:
  > cp /home/trainer/74ACT299/INIT_FILES/full_flow_2Modify /home/trainXv93/M2/74ACT299/testflow/.
- Copy the pattern file associated with this test flow to your "vectors" directory with the command:
  > cp /home/trainer/74ACT299/INIT_FILES/pattern_full_flow /home/trainXv93/M2/74ACT299/vectors/.

The levels and timing files used for this full_flow are the same than for the first_flow (levels_74ACT299, timing_74ACT299).

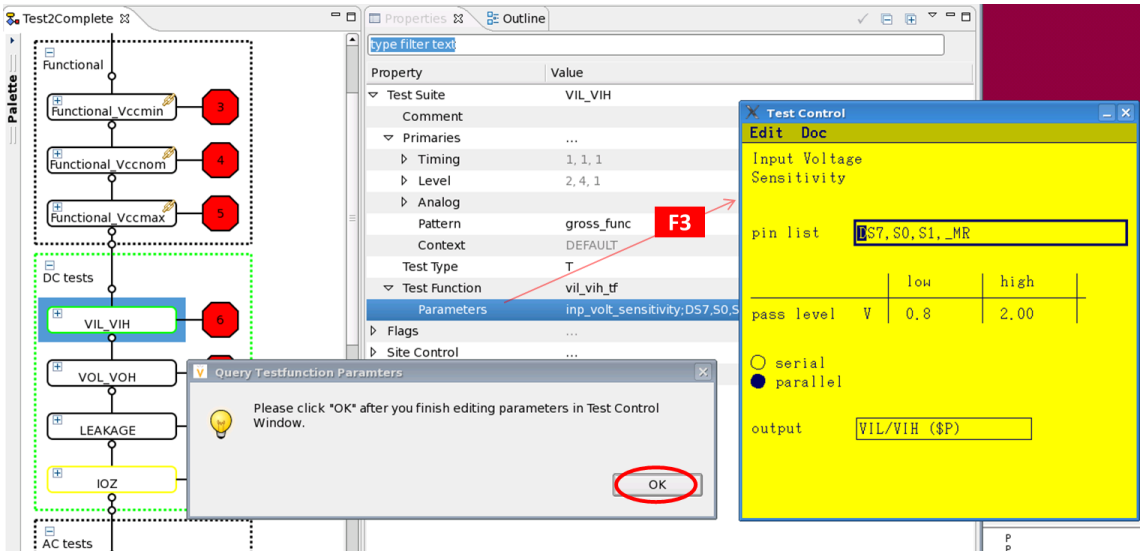
Step 2: Modify the existing test flow (offline)

- Load the test flow from the Test Program Explorer and open it in the graphical editor (Flow Sequence Editor).
- Load the primary files associated to this test flow ("Load all setups").

You have now to modify the test flow in order to specify the correct test conditions and limits for the DC and AC tests (Vil/Vih, Vol/Voh, leakage current, setup time, hold time and propagation delay).
The modification of the values will be done in the **"test control"** window (yellow window) for each test block. The procedure is the following:

- Select the first test block you want to modify.
- In the Properties window, select **"Test Function > Parameters"** and press **F3**. This will open the "test control" window.

- Change the default values by the values you have extracted from the datasheet. Don't apply any change in the pin list.
- Once the changes are done, close the "test control" window and move to the next test block in the test flow.



You have to modify the following test blocks:

- **1 Vil/Vih test**:
  only Vil and Vih values matter.
- **1 Vol/Voh test:**
  Vol/Voh + Iol/Ioh values have to be considered.
  The test control block also asks low/high limits for PMU clamp voltage; enter 0V and 5V respectively.
- **3 setup time tests**:
  - DS0/DS7 (ser_in) versus CP
  - IO[0:7] versus CP
  - S0/S1 (mode) versus CP
- **3 hold time tests**:
  - DS0/DS7 (ser_in) versus CP
  - IO[0:7] versus CP
  - S0/S1 (mode) versus CP
- **2 propagation delay tests**:
  - Q0/Q7 (ser_out) versus CP
  - IO[0:7] versus CP

Once you have modified all the test blocks, save the new test flow under the name **"full_flow"** (click right on the test flow item in the Test Program Explorer and select choose "**save as**").

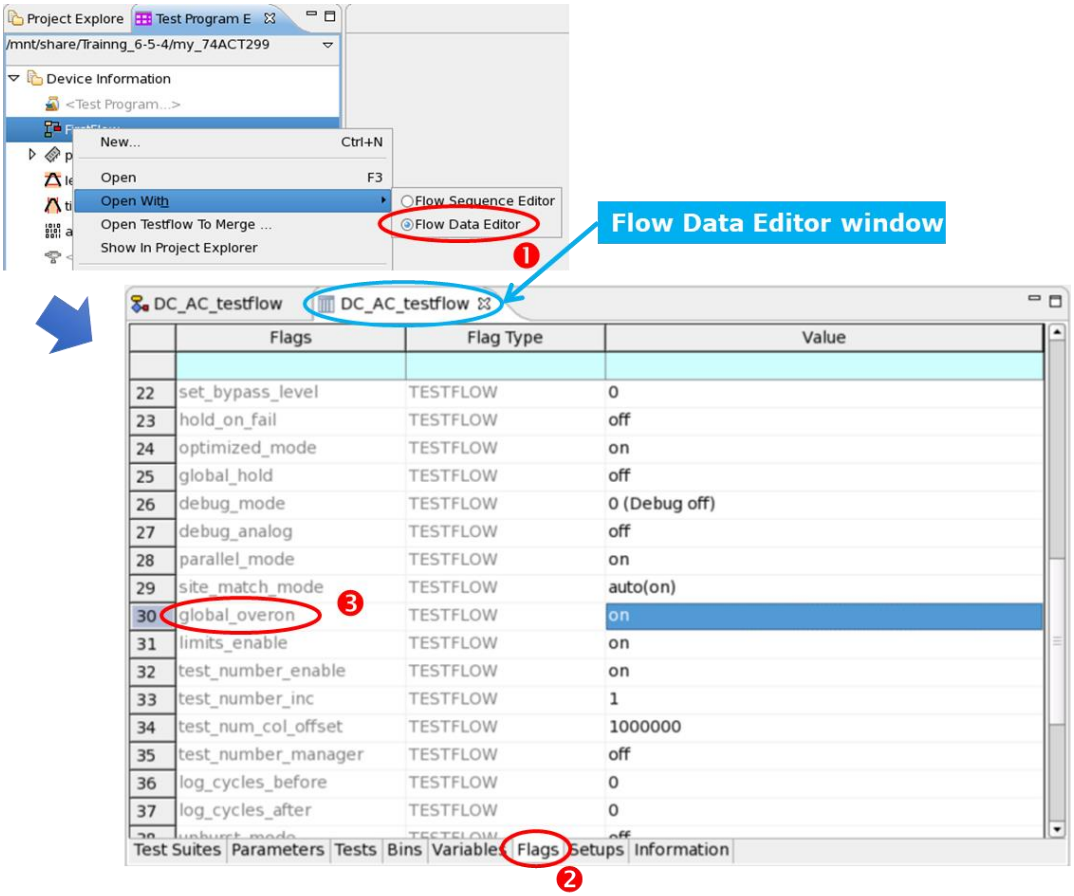
Step 3: Run the test flow (offline)

Run the test flow offline to verify that you don't have **any syntax error**.

Note: In the offline mode, a Fail might be obtained at any of the parametric tests because the simulator returns dummy values, and the test flow stops at the Fail result. In order to verify the syntax of the entire test flow, you should permit the complete execution of the test flow.

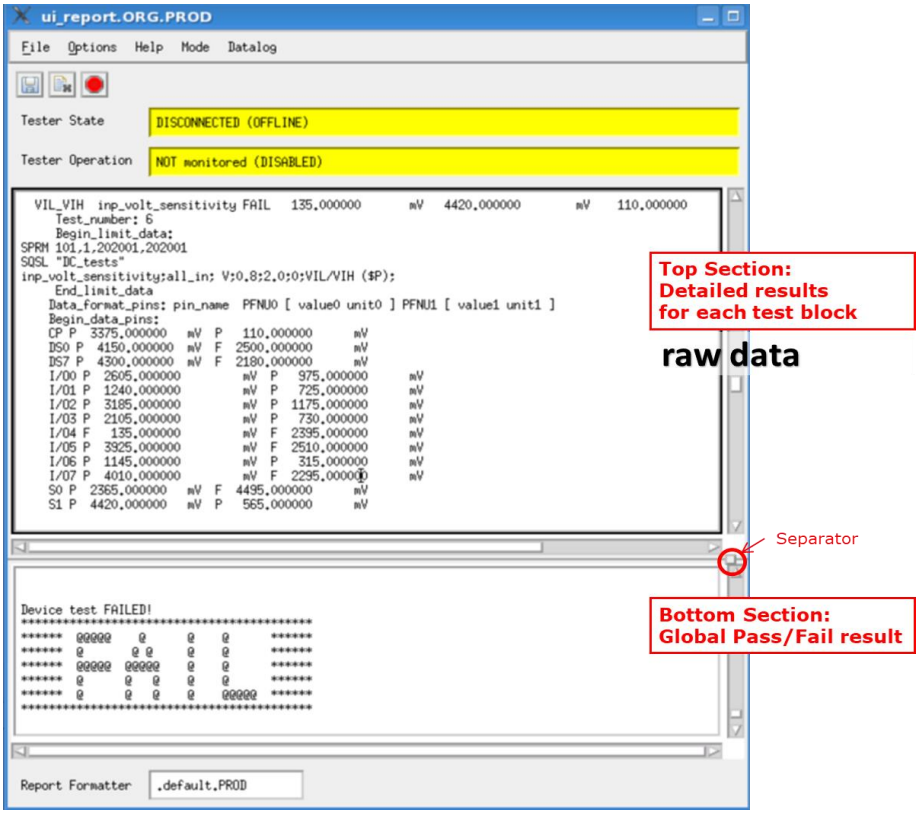
For this, perform the following actions:

- Open the test flow in the "**Flow Data Editor**" (click right on the test flow item in the Test Program Explorer and select "Open with > Flow Data Editor").
- Choose the "**Flags**" tab at the bottom of the window.
- Search the "**Global Overon**" flag and change its value it to "**on**". This will enable to continue the execution of the test flow until the final bin, even after reaching a "Bad" bin.



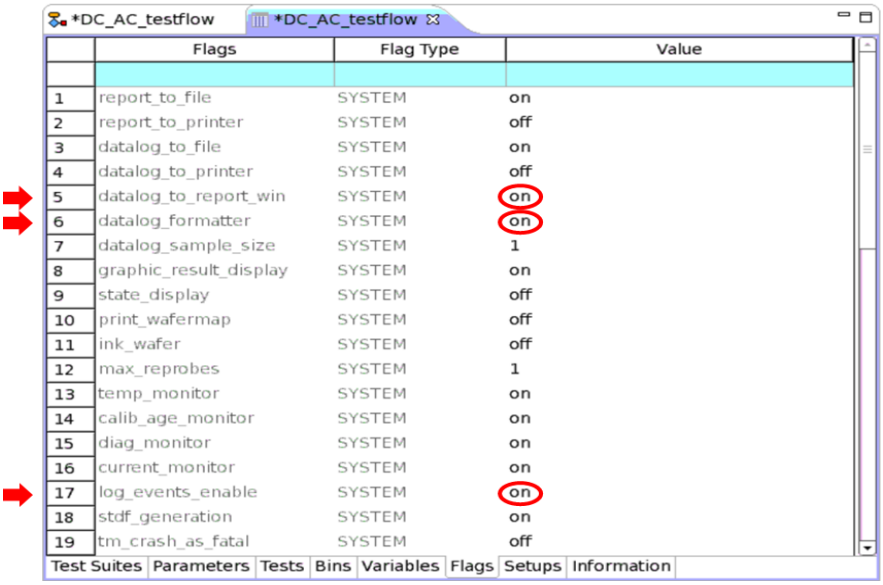
Return to the **Flow Sequence Editor** and run again the entire test flow. All test blocks are now executed, i.e. they all have a Pass or Fail result (as indicated by the green/red color of each test block).

Look at the results in the **UI-report** window. You should have two sections, the bottom section with the global Pass/Fail result and the top section with the detailed results for each test block. Separator between the 2 sections can be moved from the small square on the right side.



If you don't have the top section, perform the following actions:

- Open the test flow in the "**Flow Data Editor**" (click right on the test flow item in the Test Program Explorer, select "Open with > Flow Data Editor") and choose the "**Flags**" tab.
- Make sure that the flags "**datalog_to_report_win**", and "**datalog_formatter**" and "**log_event_enable**" are set to "**on**".
- Make sure that the flags "**datalog_to_report_win**", and "**datalog_formatter**" and "**log_event_enable**" are set to "**on**".

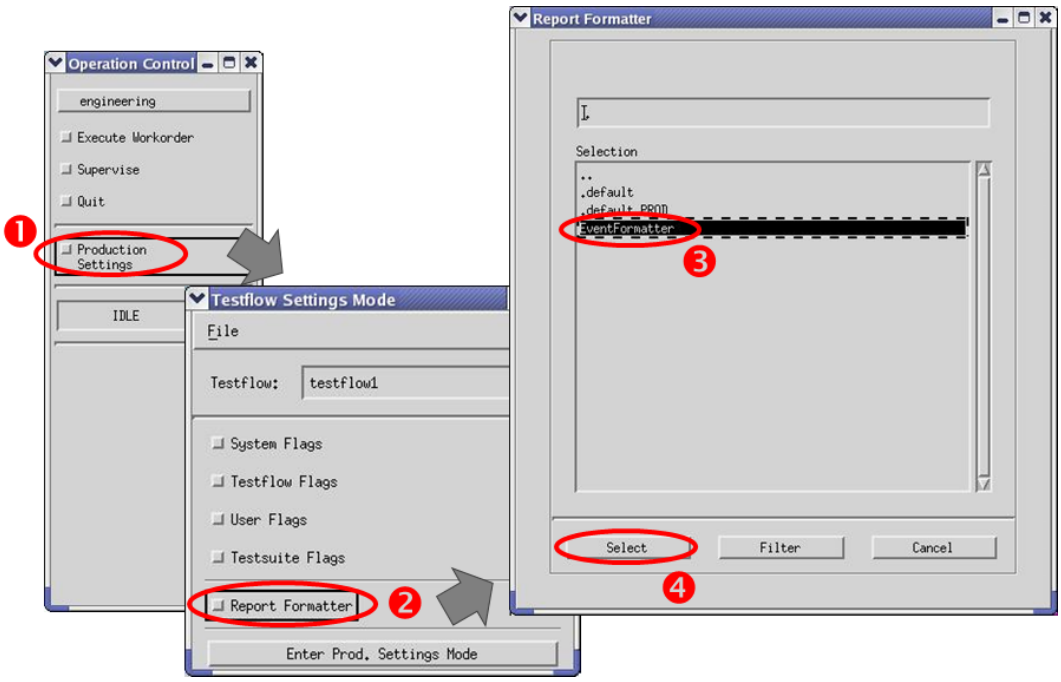


- Return to the **Flow Sequence Editor** and run again the entire test flow. You should now have the two sections.

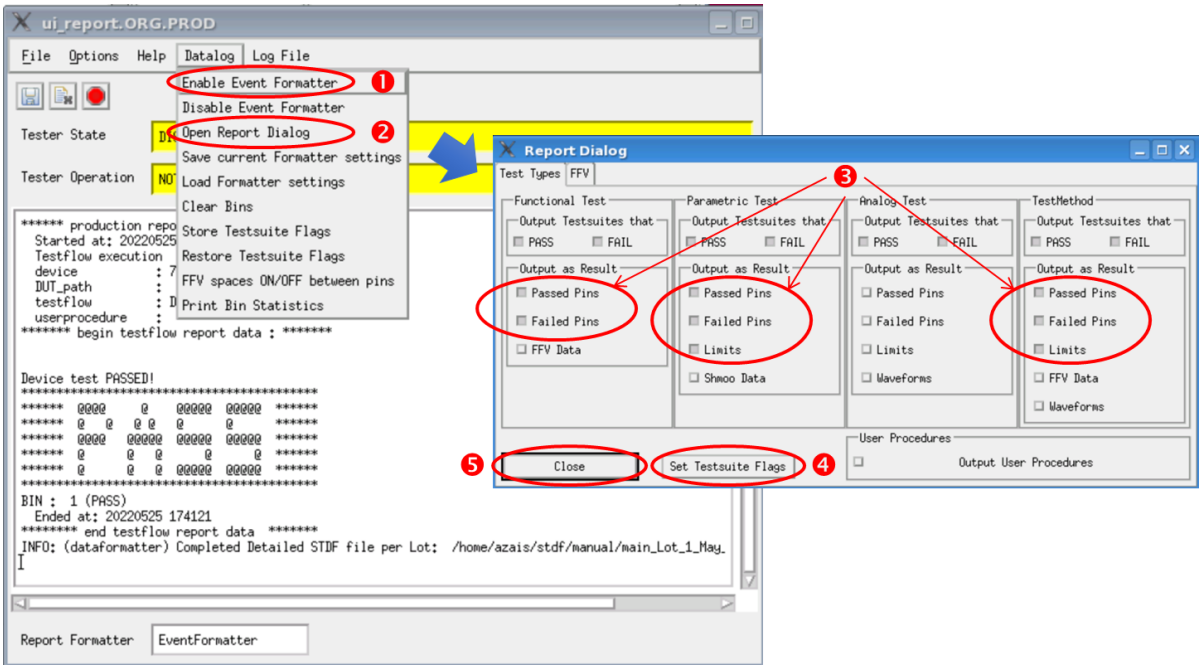
Note: The default format used to display the detailed results in the UI-report window is a raw format that does not help to data readability.

To improve data readability, you can specify the use of a formatter with the following actions:

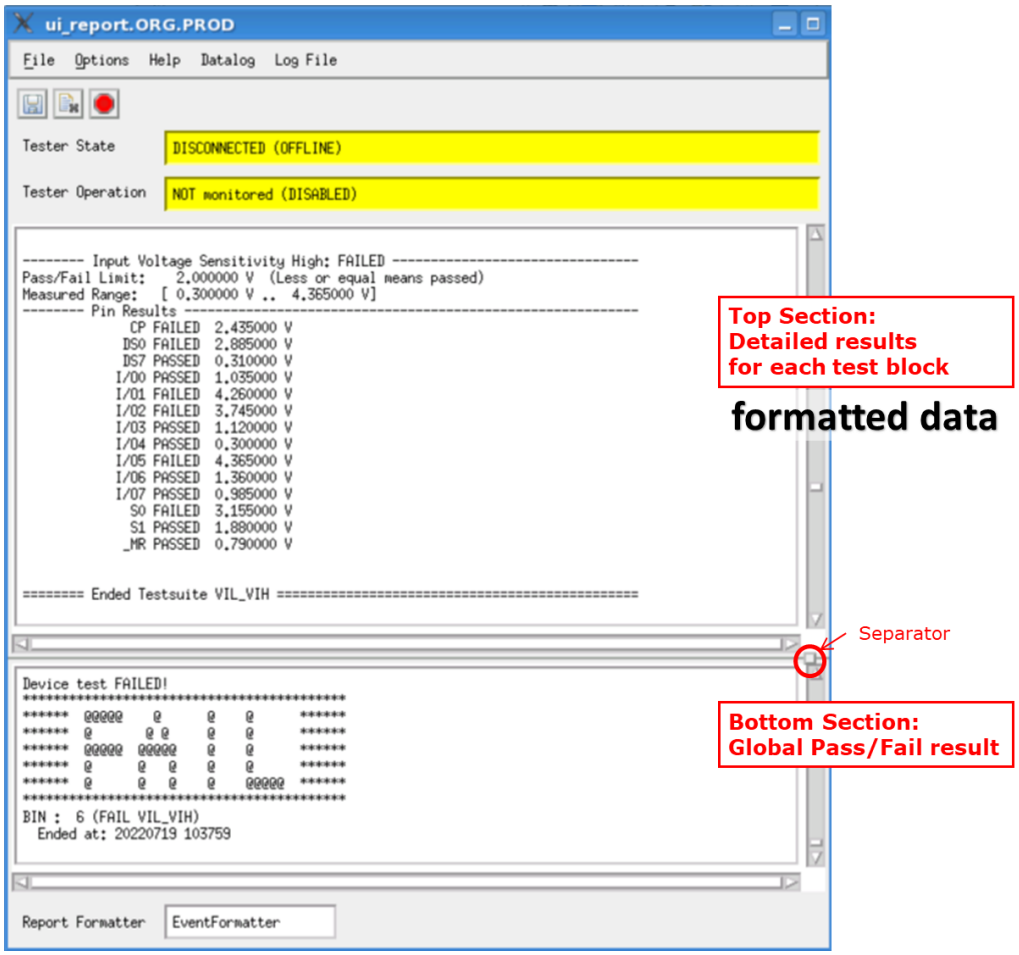
- Go to the "**Operation Control**" window. Click on "**Production Settings**", then click on "**Report Formatter**", choose "**EventFormatter**" and finish with "**Select**".



- Go to the "**UI-report**" window. In the "**Datalog**" menu, choose "**Enable Event Formatter**". Then choose "**Open Report Dialog**". For each test type (except the analog one), select "**Passed Pins**", "**Failed Pins**" and "**Limits**" (when available). Click on "**Set Testsuite Flags**" and finish with "**Close**".



- Return to the **Flow Sequence Editor** and run again the entire test flow. Look at the detailed results in the top section of the **UI_report** window. The data are now much easier to read…



Once all these steps are accomplished and everything is ok, your testflow is ready to be executed online. Quit the offline license. **Do not forget to disable the Flag "Global Overon" in the Flow Data Editor before going to the online mode.**

Step 4: Run the test flow (online)

- Connect to verigyon2016 and launch the online license.
- Load your test flow, open it in the graphical editor and load the primary files associated to this test flow ("Load all setups").
- Execute the test flow.
- Look at the global Pass/Fail result in the bottom part of the **UI-report** window. You should obtain a Pass!
- Look at the detailed results in the top part of the **UI-report** window. If data are not correctly formatted, repeat the procedure described in the preceding page to specify the use of a formatter and run again the entire test flow.
- Save the detailed results given in the top section of **UI-report** window in a text file (click in the top section and then click on menu "File > Save") and **quit the online license**.

Exercise: 74ACT299 – AC_DC_testflow – Test Results

From the analysis of the detailed results saved in the text file, write in the following table the **worst-case values** observed over the tested pins for each measurement. Evaluate the corresponding margin based on the datasheet information.

$$Margin\ (\%) = \frac{(Measured\ Value\ \pm\ DS\ Limit)}{DS\ Limit} * 100$$

Measurement	Worst-case value	Datasheet guaranteed value	Margin (%)
VIL			
VIH			
VOL			
VOH			
Setup time Ser_in to CP			
Setup time IOx to CP			
Setup time Mode to CP			
Hold time Ser_in to CP			
Hold time IOx to CP			
Hold time Mode to CP			
Propagation delay CP to Ser_out			
Propagation delay CP to IOx			

Looking at these results, what can you say about the device?

QUESTIONS ABOUT PARAMETRIC TESTS

Answer to the following questions relative to parametric tests.

Vil/Vih tests

What is the purpose of Vil/Vih test?

Observe the VIL/VIH measurements displayed in the table below.

PIN	VIL	VIH
DS7	1.500000 V	1.785000 V
S0	1.395000 V	1.825000 V
S1	1.455000 V	1.845000 V
_MR	1.435000 V	1.740000 V

According to the data sheet values, do you think these tests pass at T°=25C? Justify your answer.

Vol/Voh tests

What is the purpose of Vol/Voh test?

Referring to the datasheet, how many Vol/Voh tests should be implemented to exhaustively verify all Vol/Voh specifications? List them.

Leakage tests

Explain the condition on Vcc.

How do you manage the Iil/Iih test if you have classic input pins and pull-up ones?

Setup and hold time tests

Do you agree with both definitions?

- The setup time is the maximum amount of time the data input must be held steady before the activation of the clock.
- The hold time is the minimum amount of time that the data have to be present before the activation of the clock.

If not, provide the correct definition.

Look at setup time measurements displayed in the table below.

PIN	SETUP TIME
IO0	3.493000 ns
IO1	3.431000 ns
IO2	3.294000 ns
IO3	3.210000 ns
IO4	3.227000 ns
IO5	3.232000 ns
IO6	3.192000 ns
IO7	3.393000 ns

According to the datasheet values, do you think this test passes at T°=25C? Justify your answer.

Propagation delay tests

What is the purpose of the propagation delay test?

Do the following measurements meet the specifications?

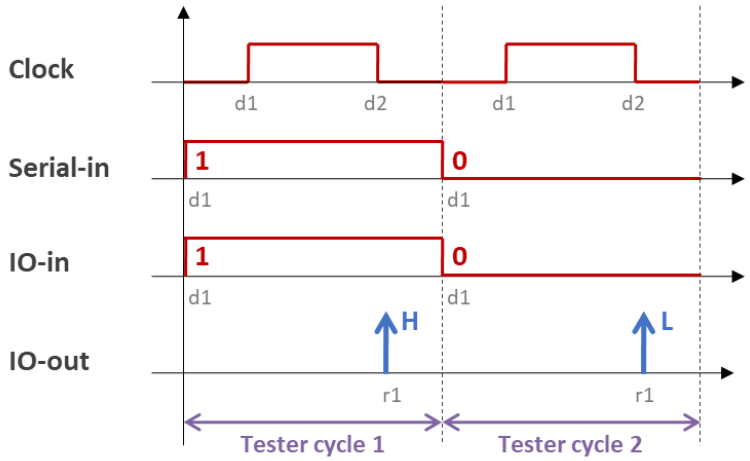
PIN	Prop delay
Q7	9.701000 ns
Q0	10.535000 ns

QUESTIONS ABOUT SHMOO PLOT ANALYSIS

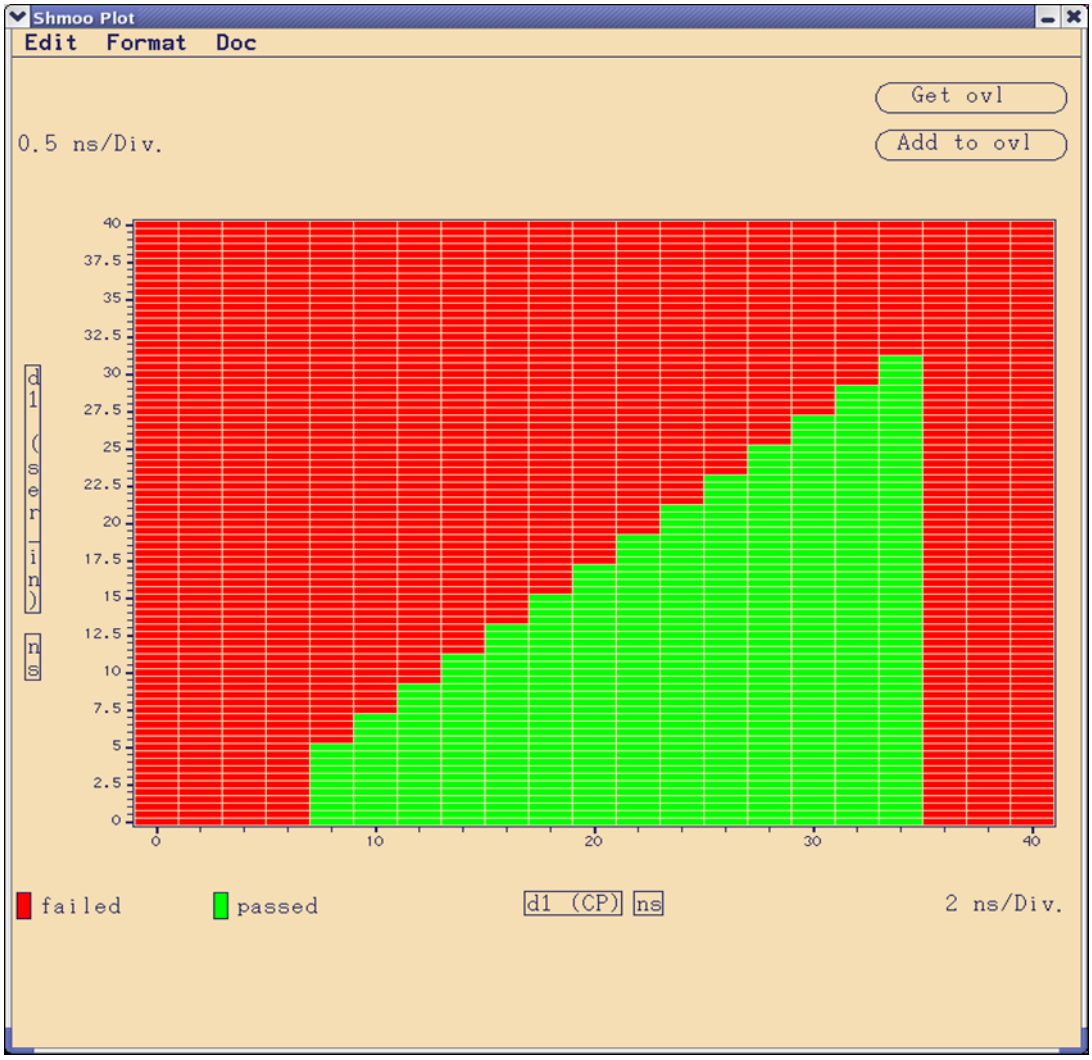
What are the objectives of performing shmoo plots?

You have to analyse the 2 shmoo plots presented hereafter using the following procedure:

1. Identify the parameters that are varied on the X and Y axis and their variation range.
2. Observe the Pass/Fail frontier and identify the threshold value of both parameters for each P/F area. Does the circuit comply with the datasheet specifications? If possible, evaluate the margin with respect to datasheet specifications.
3. Explain what the shmoo plot reveals about the circuit behavior.

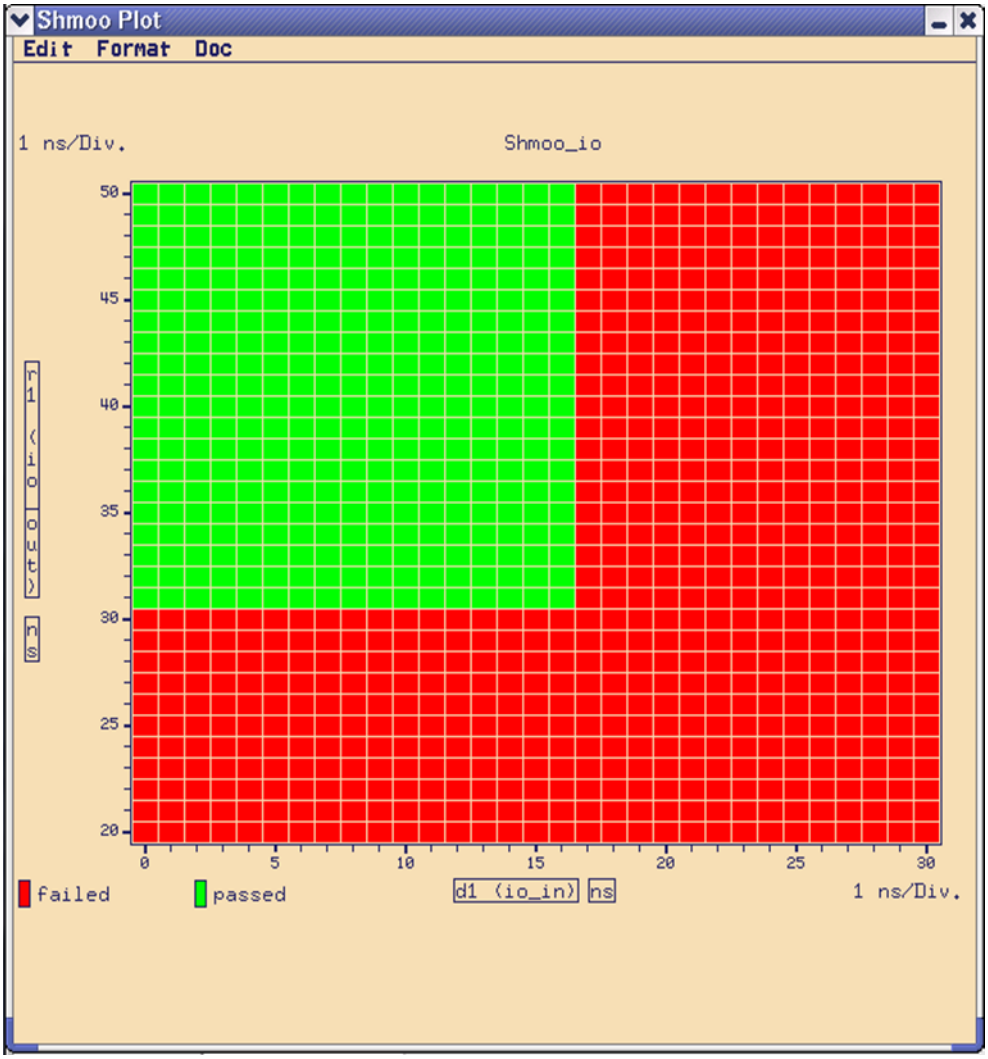


1. **Analysis of shmoo plot n° 1** (Vcc=5V)**:**



Analysis:

2. Analysis of shmoo plot n° 2 (Vcc=5V, d1-CP=20ns)**:**



Analysis:

PART 6: DEBUG & DIAGNOSIS

TEST FLOW DEBUG

In this lab, you will use the tools provided in SmarTest (Error Map, Pattern Debugger, Timing Diagram) to debug a test flow in which programming errors have been intentionally introduced.

Depending on the progress of the course, this lab will be done either by the trainees alone, or interactively with the trainer.

Step 1: Copy an existing test flow (offline)

- Open a terminal window from the RedHat menu «  ».
- Copy the test flow file called "**full_flow_2Debug**" to your testflow directory with the command:
  > **cp /home/trainer/74ACT299/INIT_FILES/full_flow_2Debug /home/trainXv93/M2/74ACT299/testflow/.**
- Copy the primary files associated with this test flow to the proper directories with the commands:
  > **cp /home/trainer/74ACT299/INIT_FILES/levels_2Debug /home/trainXv93/M2/74ACT299/levels/.**
  > **cp /home/trainer/74ACT299/INIT_FILES/timing_2Debug /home/trainXv93/M2/74ACT299/timing/.**
  > **cp /home/trainer/74ACT299/INIT_FILES/pattern_2Debug /home/trainXv93/M2/74ACT299/vectors/.**

Step 2: Run and debug the test flow (online)

- Connect to verigyon2016 and launch the online license.
- Load the test flow, open it in the graphical editor and load the primary files (pins_103, levels_2Debug, timing_2Debug, pattern_2Debug).
- Run and debug the test flow using any tool available in SmarTest. After your modifications, you should obtain a Pass!

Results – Test Flow Debug

Detail your observations and modifications in the following table.

Failing Testsuite Name	Identified Problem	Correction

Exercise: FOCUS ON FAULT DIAGNOSIS

In this section, faults have been inserted in the device using the FPGA board approach. Using the pattern debugger tool of the tester, we have collected the resulting failing cycles and failing pins in the test pattern. Each red box corresponds to a failing cycle + failing output pin. The value in the box corresponds to the expected data on the output pin, not the captured one.

From the given pattern reports and without using any tool, found the type of fault (stuck at 0 or 1) and the faulty pin. Each pattern report corresponds to a single stuck at fault introduced on one of the following pins: IO/1, IO/5, IO/6, DS0, DS7, S0, S1 and CP.

Fill the following table with your results. For each pattern report, detail your analysis (Observation > Hypothesis > Conclusion).

Pattern Report	Stuck-at-1	Stuck-at-0	Faulty pin
Pattern report n°1			
Pattern report n°2			
Pattern report n°3			
Pattern report n°4			
Pattern report n°5			

Pattern report n° 1

		Signal	CLK_IN	CLK_IO	_MR	CP	SO	S1	DSO	DS7	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Q0	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	H	L	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	H	H	L	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

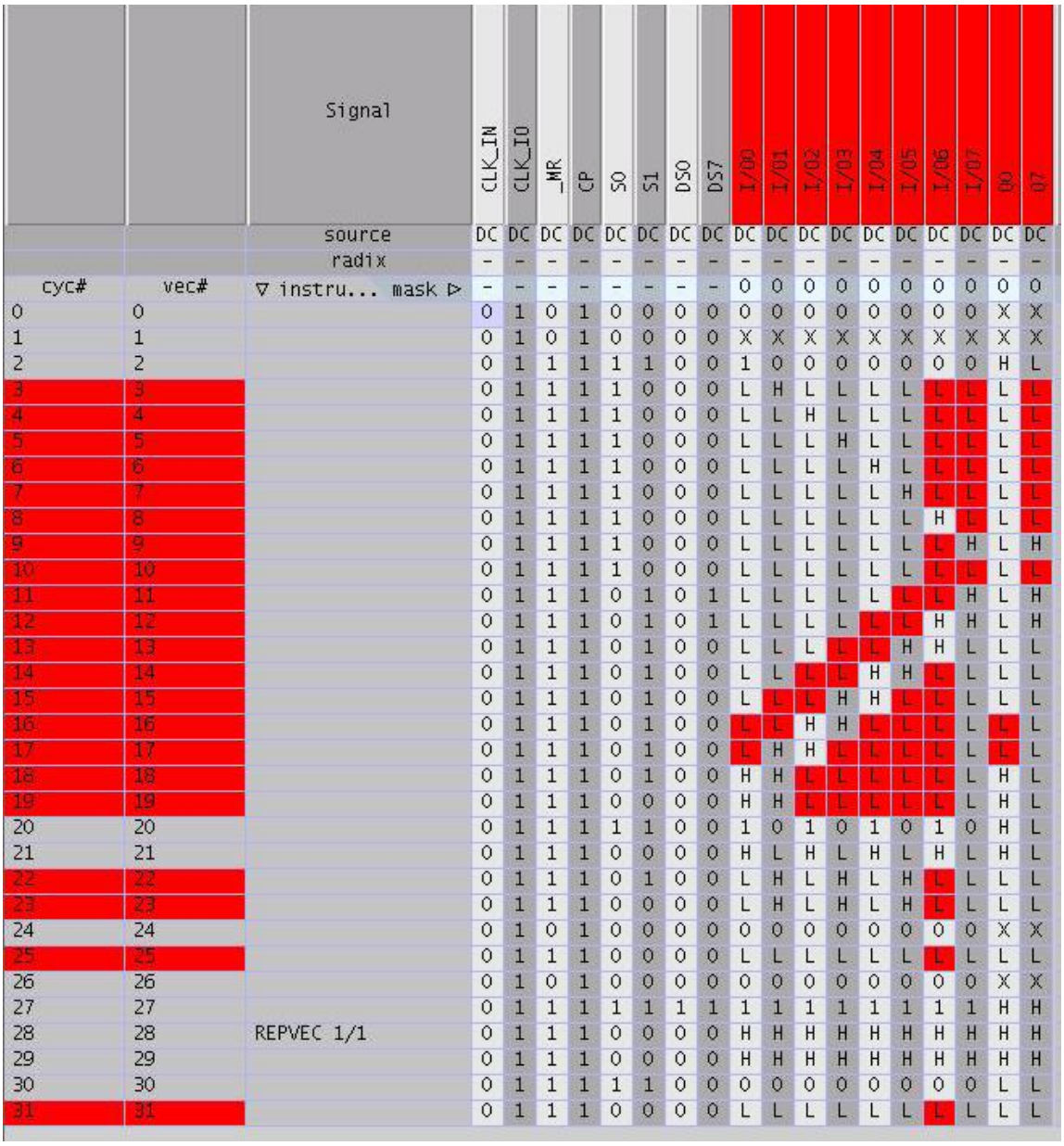
Analysis:

Pattern report n° 2

		Signal	CLK_IN	CLK_IO	_MR	CP	SO	S1	DSO	DS7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07	QO	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	H	L	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	H	H	L	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

Analysis:

Pattern report n° 3



		Signal	CLK_IN	CLK_IO	_MR	CP	SO	S1	DSO	DS7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07	Q0	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	H	L	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	H	H	L	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

Analysis:

Pattern report n° 4

		Signal	CLK_IN	CLK_IO	_MR	CP	S0	S1	DS0	DS7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07	Q0	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	H	L	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	H	H	L	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

Analysis:

Pattern report n° 5

		Signal	CLK_IN	CLK_IO	_MR	CP	S0	S1	DS0	DS7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07	Q0	Q7
		source	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
		radix	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cyc#	vec#	▽ instru... mask ▷	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0
0	0		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
1	1		0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X
2	2		0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	H	L
3	3		0	1	1	1	1	0	0	0	L	H	L	L	L	L	L	L	L	L
4	4		0	1	1	1	1	0	0	0	L	L	H	L	L	L	L	L	L	L
5	5		0	1	1	1	1	0	0	0	L	L	L	H	L	L	L	L	L	L
6	6		0	1	1	1	1	0	0	0	L	L	L	L	H	L	L	L	L	L
7	7		0	1	1	1	1	0	0	0	L	L	L	L	L	H	L	L	L	L
8	8		0	1	1	1	1	0	0	0	L	L	L	L	L	L	H	L	L	L
9	9		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	H	L	H
10	10		0	1	1	1	1	0	0	0	L	L	L	L	L	L	L	L	L	L
11	11		0	1	1	1	0	1	0	1	L	L	L	L	L	L	L	H	L	H
12	12		0	1	1	1	0	1	0	1	L	L	L	L	L	L	H	H	L	H
13	13		0	1	1	1	0	1	0	0	L	L	L	L	L	H	H	L	L	L
14	14		0	1	1	1	0	1	0	0	L	L	L	L	H	H	L	L	L	L
15	15		0	1	1	1	0	1	0	0	L	L	L	H	H	L	L	L	L	L
16	16		0	1	1	1	0	1	0	0	L	L	H	H	L	L	L	L	L	L
17	17		0	1	1	1	0	1	0	0	L	H	H	L	L	L	L	L	L	L
18	18		0	1	1	1	0	1	0	0	H	H	L	L	L	L	L	L	H	L
19	19		0	1	1	1	0	0	0	0	H	H	L	L	L	L	L	L	H	L
20	20		0	1	1	1	1	1	0	0	1	0	1	0	1	0	1	0	H	L
21	21		0	1	1	1	0	0	0	0	H	L	H	L	H	L	H	L	H	L
22	22		0	1	1	1	0	1	0	0	L	H	L	H	L	H	L	L	L	L
23	23		0	1	1	1	0	0	0	0	L	H	L	H	L	H	L	L	L	L
24	24		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
25	25		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L
26	26		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X
27	27		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	H	H
28	28	REPVEC 1/1	0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
29	29		0	1	1	1	0	0	0	0	H	H	H	H	H	H	H	H	H	H
30	30		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	L	L
31	31		0	1	1	1	0	0	0	0	L	L	L	L	L	L	L	L	L	L

Analysis: